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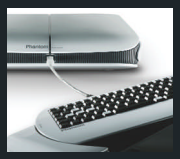



# WIRELESS-SENSOR NETWORKS

## FIND A FIT IN THE UNLICENSED BAND

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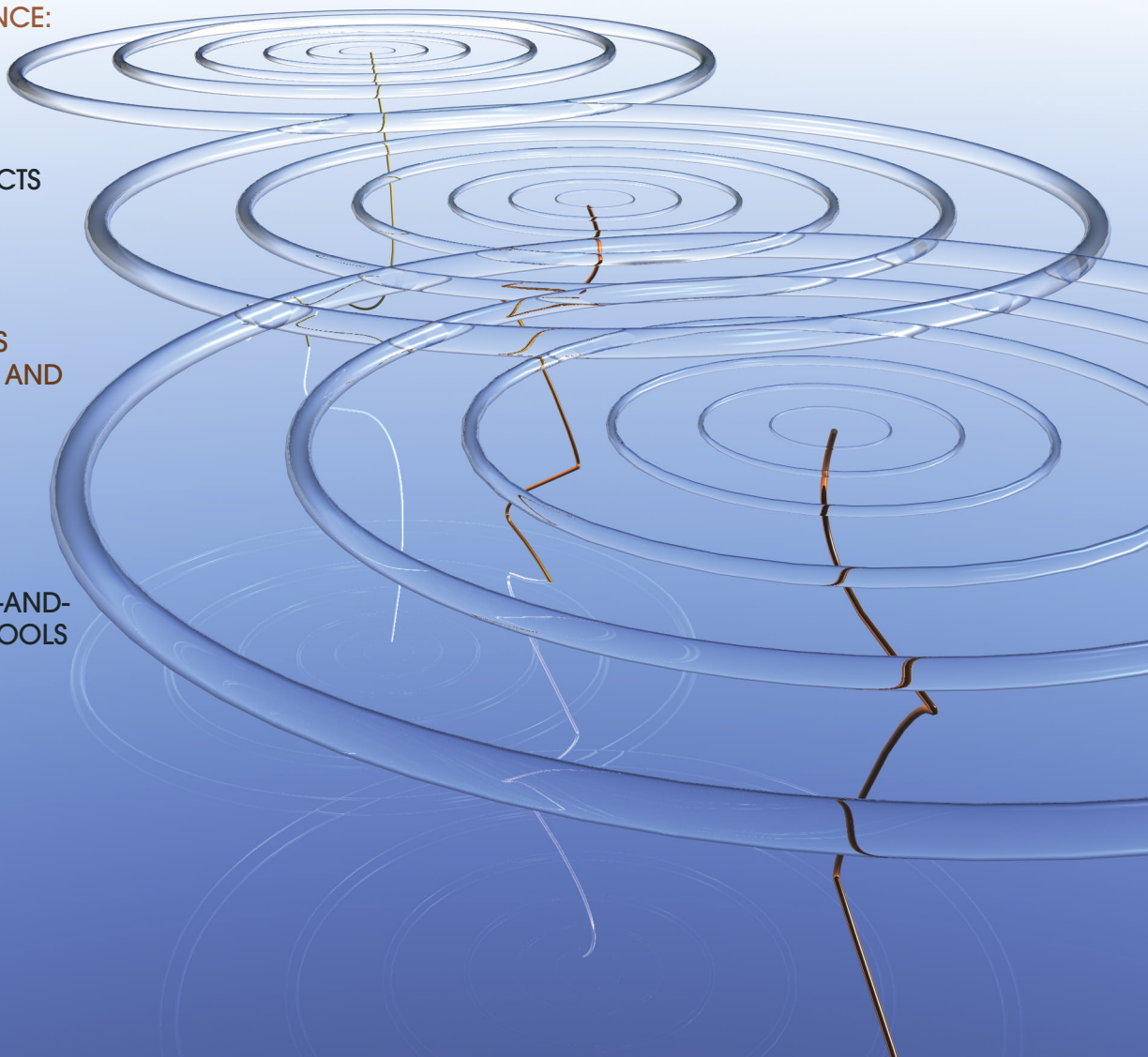

# High Frequency 2.5MHz ROHM Switching Regulators

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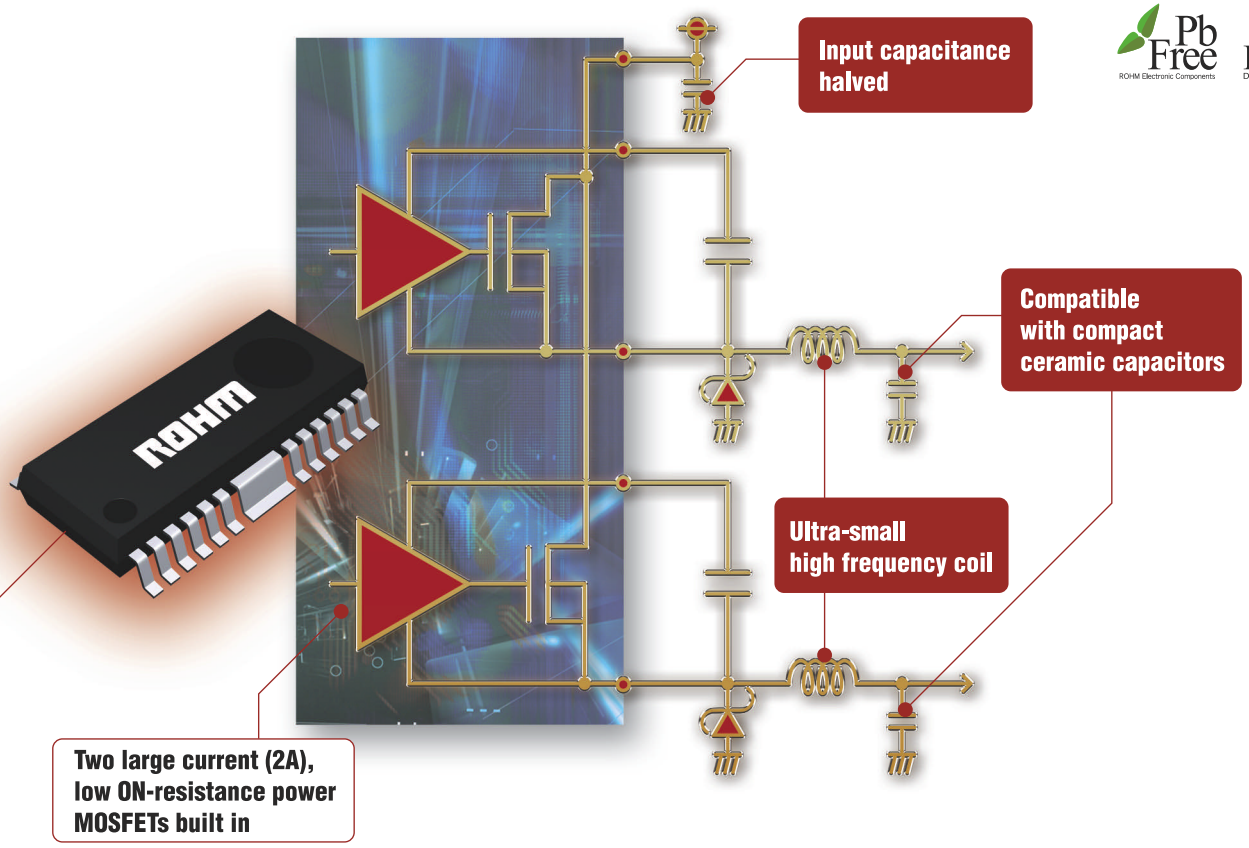


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**BD9302FP**

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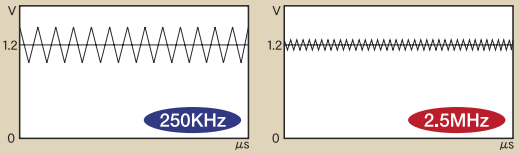
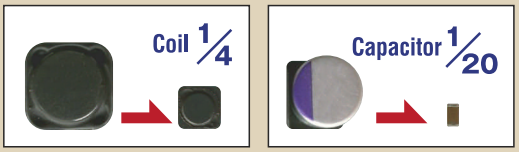



Compatible with smaller external coil and capacitor




*The above advantages are not applicable at the same time.

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| Type | Part Number | Supply Voltage(V) | Output Current(A) | Output Voltage(V) |
|---|---|---|---|---|
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| | BD9703 series | 8 to 35 | 1.5 | 1 to Vcc-3 |
| | BD9702 series | 8 to 35 | 3 | 1 to Vcc-3 |
| Flexible step-down | BD9001F | 7 to 46 | 2 | 1 to VIN |
| | BD9778 series | 5 to 35 | 2 | 1 to VIN |
| | BD9781HFP | 5 to 35 | 4 | 1 to VIN |
| High-efficiency step-down | BD9106FVM | 4.0 to 5.5 | 0.8 | 1 to 2.5 |
| | BD9109FVM | 4.5 to 5.5 | 0.8 | 3.3 |
| | BD9107FVM | 4.0 to 5.5 | 1.2 | 1 to 1.5 |
| High-efficiency step-up | BD8158FVM | 2.1 to 4 | 1.4 | Vcc to 14 |
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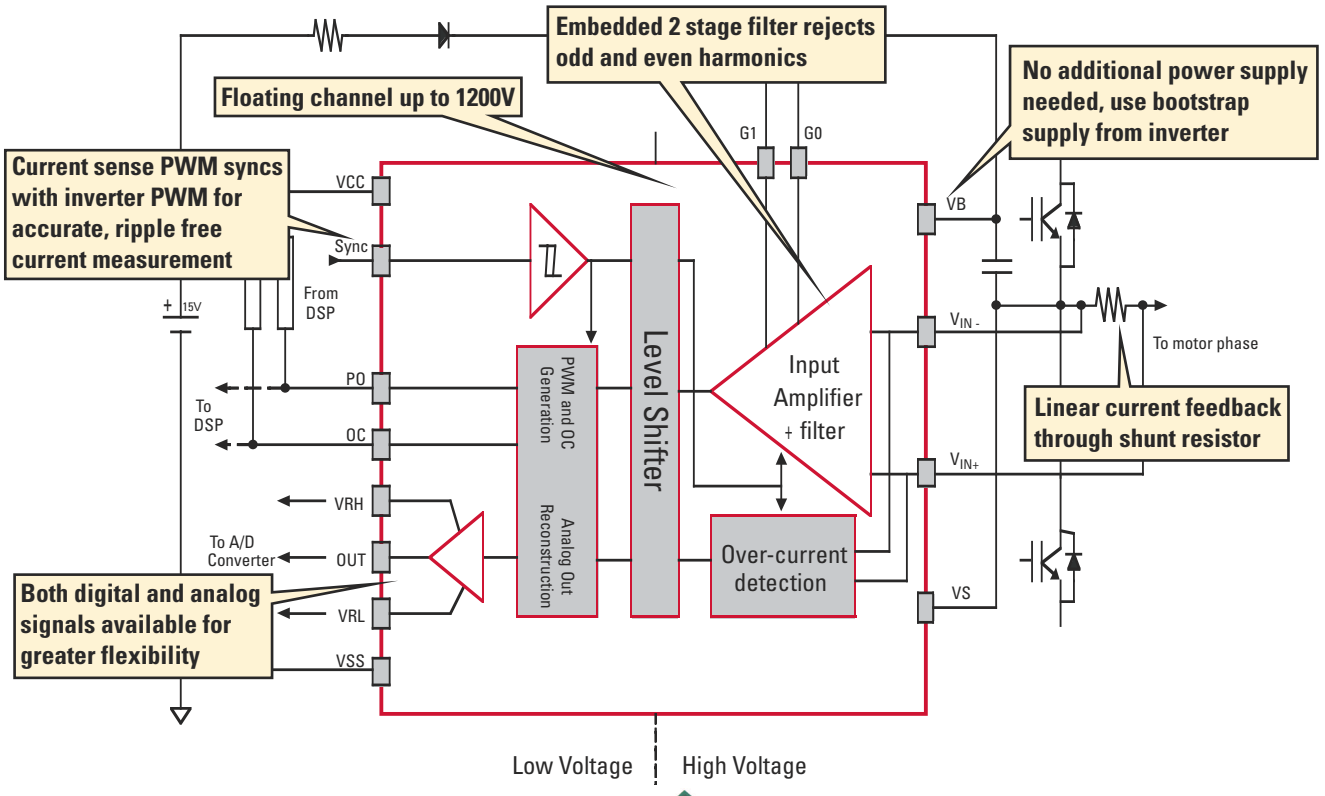


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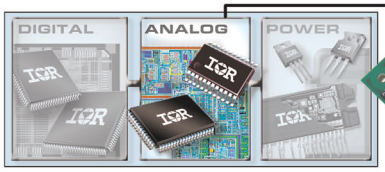


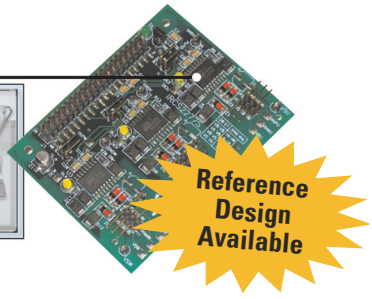


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| Carrier output frequency bandwidth | 15kHz | 20kHz | 20kHz |
| Over-current threshold | +/-260mV | +/-470mV | +/-470mV |
| Analog output dynamically adjustable | N/A | Yes | Yes |
| Package | 8-pin SOIC | 16-pin SOIC | 16-pin SOIC |
| 2-Stage filter | No | Yes | Yes |
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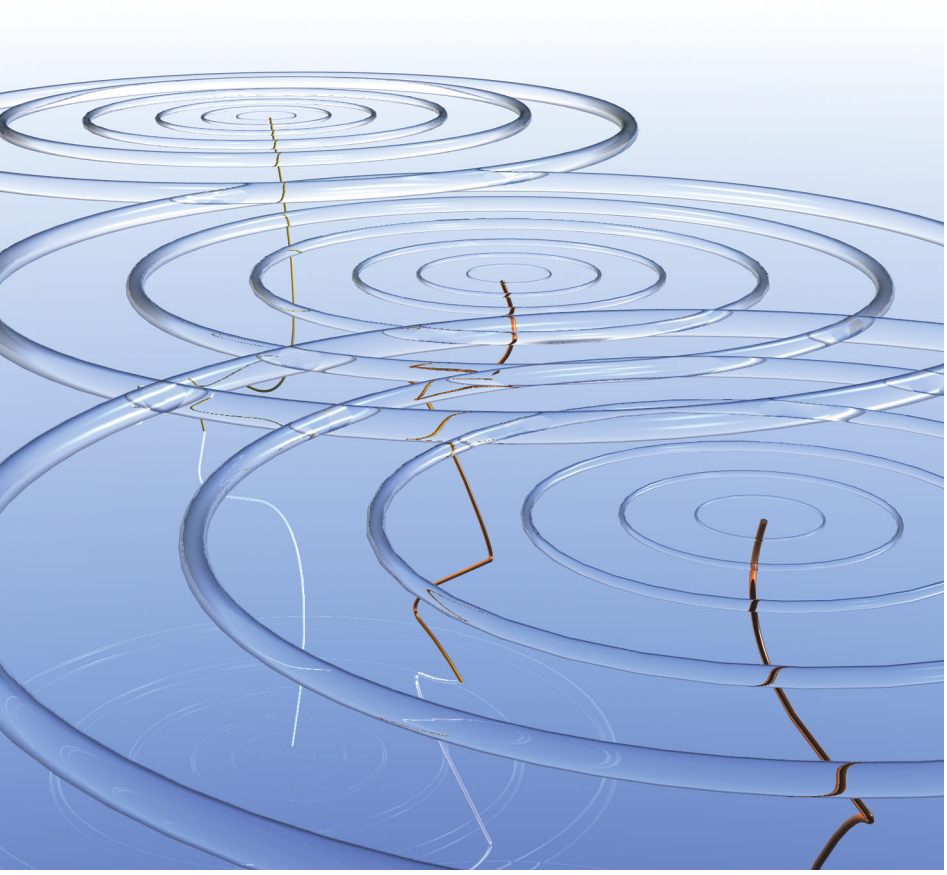

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50 years

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3.16.06

## Wireless-sensor networks find a fit in the unlicensed band



## ROHS compliance: It's not easy being green



## System architects get help from emulators



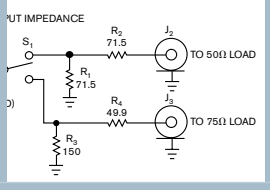
## The economics of structured- and standard-cell-ASIC designs



## Mobile applications challenge test-and-measurement tools



# DESIGNIDEAS



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## pulse

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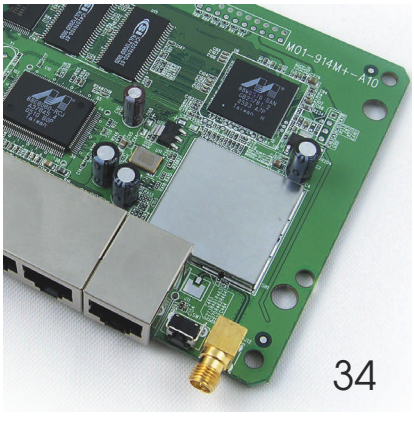

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## DEPARTMENTS & COLUMNS



## PRODUCT ROUNDUP




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DESIGN idea

# Intermediate Frequency (IF) Sampling Receiver Concepts

*Mark Rives, Principal Applications Engineer*

This article will discuss Intermediate Frequency (IF) sampling concepts of sub-sampling (or under sampling), noise processing gain, and the effects of interfering signals. Examples will be based on the GSM/EDGE communications standard where the channel bandwidth is 200 kHz and the sample rate is typically a multiple of 13 MHz.

## Sub-Sampling

Nyquist's sampling theorem states that if a signal is sampled at least twice as fast as the highest sampled frequency component, no information will be lost when the signal is reconstructed. The sample rate divided by two (Fs/2) is known as the Nyquist frequency and the frequency range from DC (or 0 Hz) to Fs/2 is called the first Nyquist zone.

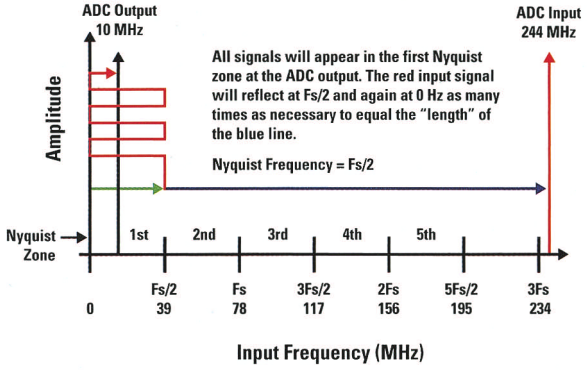



**Figure 1. Nyquist Sampling Example**

We'll use National's high-speed ADC12DL080 as an example. Clocking the ADC12DL080 at 6 * 13 MHz or 78 Mega-Samples Per Second (MSPS) places the Nyquist frequency at 39 MHz. All the signal information that falls in the first Nyquist zone is over sampled and can be recovered. If the sampled signal moves into the second Nyquist zone from 39 MHz to 78 MHz, it can still be recovered but the absolute frequency information is lost. When the input signal moves above Fs/2, it has been sub-sampled and 'reflects' or 'folds' at Fs/2 and moves back toward 0 Hz at the ADC output. If Fs/2 = 39 MSPS, an input signal at 40 MHz will fold back to 38 MHz. Folding will occur in each Nyquist zone. For example, a 244 MHz IF at 78 MSPS will result in a 10 MHz signal at the ADC output. The folded (or aliased) frequency is calculated by finding the closest multiple of Fs to the desired input frequency ($F_{IN}$, 244 MHz), then subtracting the two frequencies:

$$F_{IN} = (n * Fs) \text{ or } 244\ MHz - (3 * 78\ MHz)$$
$$= 244\ MHz - 234\ MHz = 10\ MHz$$

Signals at 10 MHz, 68 MHz, 88 MHz, 146 MHz, and beyond will all appear at 10 MHz. There is no way to determine the original IF since the Nyquist criteria has been violated.

Sub-sampling systems take advantage of this folding or mixing function to reduce the IF frequency prior to a final digital tuner like National's CLC5903. If the desired signal Bandwidth (BW) is less than Fs/2, all of the signal information can still be recovered. A channel filter should be placed in front of the ADC to remove any undesired signals from other Nyquist zones. This filter will also limit the amount of noise at the ADC input to only one Nyquist zone.

## Noise Processing Gain

As the ADC input frequency increases, the Signal-to-Noise Ratio (SNR) for large signals will decrease due to clock jitter. Small signal SNR is not affected. For the ADC12DL080, the large signal SNR will be 65 dBFS (dB relative to Full Scale) at a 244 MHz IF. When the

**NEXT ISSUE:**
**Extending Power-over-Ethernet**

National Semiconductor

# Featured Products

## ADC12DL080 Dual, 12-bit, 80 MSPS Analog-to-Digital Converter for High-IF Sampling

The ADC12DL080 is a dual, low-power monolithic CMOS analog-to-digital converter. This device is capable of converting an analog input signal into 12-bit digital words at rates up to 80 Mega-Samples Per Second (MSPS). The ADC12DL080 is designed with 600 MHz full-power input bandwidth and low aperture jitter to allow sampling of high-frequency IF inputs. Operating on a single 3.3V supply, the ADC12DL080 achieves 11.0 effective bits at Nyquist and consumes just 450 mW at 80 MSPS. A power-down feature reduces power consumption to 100 mW.

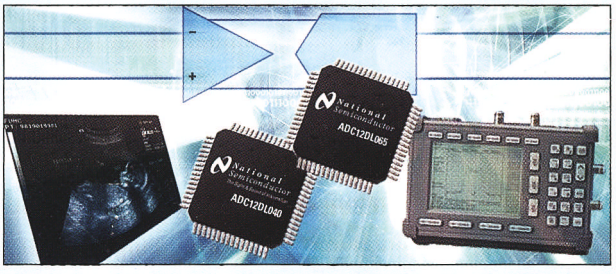

The ADC12DL080 may be used either with an external reference voltage (1.0V nominal, 0.8V to 1.5V allowed) or with an internal precision 1.0V reference. The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

### Features

- Single 3.3V supply operation
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Power-down mode
- Duty cycle stabilizer
- External or internal selectable reference
- Pin-compatible with ADC12DL040, ADC12DL065, and ADC12DL066

For input frequencies as high as 200 MHz, the ADC12DL080 provides an impressive 67 dB SNR and 81 dB SFDR, making it ideal for high-IF sampling receivers, test and measurement equipment, radar, and medical imaging applications. The ADC12DL080 is offered in a TQFP-64 package and operates over the industrial temperature range of -40°C to +85°C.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/DC/ADC12DL080.html**




## ADC12DL040/65 Dual, 12-Bit A/D Converters for Excellent Signal Conditioning and Acquisition

The ADC12DL040 and ADC12DL065 are dual, low-power 12-bit Analog-to-Digital Converters (ADC) capable of converting analog input signals at 40 and 65 Mega-Samples Per Second (MSPS), respectively. These ADCs provide excellent dynamic performance and 250 MHz full-power bandwidth. The ADC12DL040 achieves 11.1 effective bits and consumes just 210 mW at 40 MSPS and the ADC12DL065 achieves 11.0 effective bits and consumes 360 mW at 65 MSPS.

The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. The digital outputs from the two ADCs are available on a single multiplexed 12-bit bus or on two separate buses. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

### Features

- Single 3.0V (ADC12DL040) and 3.3V (ADC12DL065) supply operation
- Internal reference
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Power-down mode
- Duty cycle stabilizer
- Multiplexed output mode

The ADC12DL040/65 provide an impressive 68.5 dB SNR and 85 dB SFDR at Nyquist while consuming just 210 mW and 360 mW, respectively. These converters are ideal for portable instrumentation, medical imaging, communications receivers, and wireless infrastructure equipment. These ADCs are available in TQFP-64 packaging and operate over the industrial temperature range of -40°C to +85°C.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/DC/ADC12DL040.html**
**www.national.com/pf/DC/ADC12DL065.html**

## IF Sampling Receiver Concepts

input is reduced to -10 dBFS or less, the SNR will increase to 70 dBFS. If the desired channel bandwidth is over sampled, a digital channel filter can further improve the SNR. When an ADC's SNR is measured, it is normally specified as the SNR in the first Nyquist zone. In other words, all the noise from DC to Fs/2 is summed to get the SNR relative to the ADC's full-scale input. A digital channel filter can remove the ADC output noise except in the channel bandwidth. The output noise is integrated over a smaller frequency range. This improvement is called noise processing gain and can be calculated with the following equation:

Processing Gain = -10 * LOG (Channel BW/Nyquist BW)

For a 200 kHz narrow-band system:

Processing Gain = -10 * LOG (200 kHz/39 MHz) = 22.9 dB

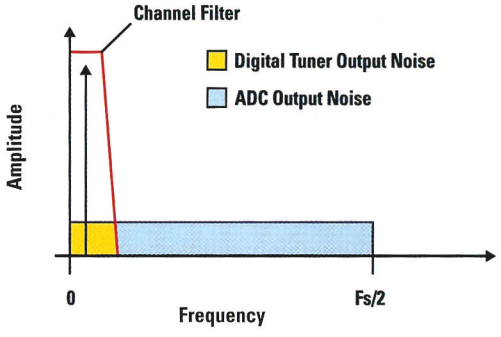



**Figure 2. Noise Processing Gain**

Processing gain can also be calculated by finding the noise floor of the ADC in dBm/Hz. With an IF of 244 MHz at -1 dBFS, the SNR of the ADC12DL080 is 65 dBFS or -55 dBm since full scale is +10 dBm into 50Ω. To translate into dBm/Hz, take 10 * LOG (Fs/2) and subtract it from -55 dBm. 10 * LOG (39 MHz) = 75.9 dB, therefore the ADC12DL080 noise floor in this example is -130.9 dBm/Hz. Now if the channel bandwidth is 200 kHz, add back 10 * LOG (200 kHz) or 53 dB to get a noise floor of -77.9 dBm in 200 kHz, which is 22.9 dB better than the ADC by itself. Translating back to dBFS, the total SNR is 87.9 dB in a 200 kHz channel. This is similar to decreasing the resolution bandwidth on a spectrum analyzer; the noise floor has been lowered, but the ADC's resolution has not been increased.

### Interfering Signals

GSM systems require the receiver to operate with signals from -13 dBm to -104 dBm when there are no interfering signals. Typical receivers need some extra margin to demodulate the received signal. This is called the Carrier-to-Interferer (C/I) ratio and is 9 dB for GSM. This means that the noise floor must be below -113 dBm, resulting in a dynamic range of greater than 100 dB, which is more than our ADC can provide. Normally a Variable Gain Amplifier (VGA) is added to the system to scale the input signal to the ADC.

Adding a VGA works well until a large interfering signal is present. In GSM systems, this condition can occur when one subscriber is close to the basestation and one is far away. The close subscriber may actually be talking to a more distant basestation on an adjacent channel, which can block the reception of the weak signal. Hence, the large signal is known as a blocker. The blocker can be up to -13 dBm while the weak signal can be as low as -101 dBm. Considering the 9 dB C/I ratio, the overall dynamic range requirement is now -13 dBm – ( -110 dBm) or 97 dB with a blocking signal. If the blocker causes the VGA gain to decrease to prevent clipping the ADC input, the weak signal can be lost in the noise.

The channel filter in front of the ADC will reduce the level of the blocking signal, but the ADC will still operate near full scale. Clock jitter and the large signal will degrade the SNR causing a loss of sensitivity if the filter rejection of the blocker is not sufficient.

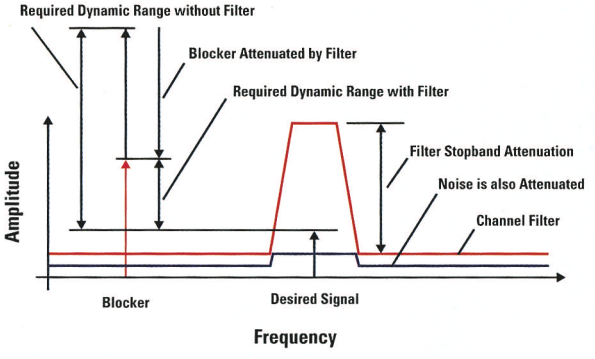


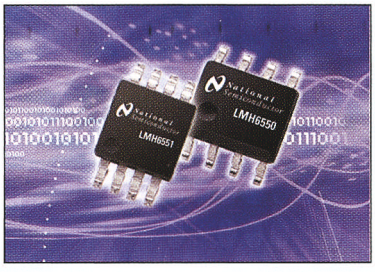

**Figure 3. Channel Filter**

### Summary

High-speed ADCs such as the ADC12DL080 combined with a digital tuner such as the CLC5903 can simplify receiver design and provide excellent performance for high dynamic range signals. More information on this topic is available in the user's guide for the CLC-LDRCS-PCASM evaluation board at www.national.com/store#DataAcquisition. ■

# Featured Products

## Differential, High-Speed Op Amps




The LMH6550 and LMH6551 are high-performance voltage feedback differential amplifiers. The fully differential topology allows balanced inputs to the ADCs and can be used as single-ended-to-differential or used as differential-to-differential. These amplifiers also have the high speed and low distortion necessary for driving high-performance ADCs, as well as the current-handling capability to drive signals over balanced transmission lines like CAT-5 data cables.

With external gain set resistors, the LMH6550/51 can be used at any desired gain. Gain flexibility coupled with high speed makes these amplifiers suitable for use as IF amplifiers in high-performance communications equipment.

### LMH6550 Features

- 400 MHz, -3 dB Bandwidth ($V_{OUT}$ = 0.5 $V_{P-P}$)
- 90 MHz, 0.1 dB Bandwidth
- -92/-103 dB HD2/HD3 at 5 MHz
- 3000 V/µs Slew rate
- -68 dB Balance error ($V_{OUT}$ = 1.0 $V_{P-P}$, 10 MHz)
- 10 ns Shutdown/enable

### LMH6551 Features

- 370 MHz, -3 dB Bandwidth ($V_{OUT}$ = 0.5 $V_{P-P}$)
- 50 MHz, 0.1 dB Bandwidth
- -94/-96 dB HD2/HD3 at 5 MHz
- 2400 V/µs Slew rate
- -70 dB Balance error ($V_{OUT}$ = 0.5 $V_{P-P}$, 10 MHz)
- Single +3.3V, +5V, or ±5V supply voltages

The LMH6550/51 are ideal for use in applications requiring a differential A/D driver, video twisted pair, differential line driver, single-ended-to-differential converter, high-speed differential signaling, IF/RF amplifier, or SAW filter buffer/driver.

The LMH6550/51 are available in the space-saving SOIC-8 and MSOP-8 packaging.

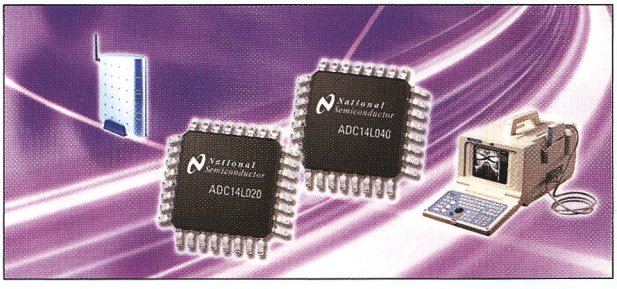
For FREE samples, datasheets, and more, visit
**www.national.com/pf/LM/LMH6550.html**
**www.national.com/pf/LM/LMH6551.html**

## ADC14L020/40 14-Bit, 20 and 40 MSPS ADCs

The ADC14L020 and the ADC14L040 are low-power, monolithic 14-bit 20 and 40 Mega-Samples Per Second (MSPS) Analog-to-Digital Converters (ADC). These ADCs provide excellent dynamic performance and 150 MHz full-power bandwidth. The ADC14L020 achieves 12.0 effective bits and consumes 150 mW at 20 MSPS. The ADC14L040 achieves 11.9 effective bits and consumes 235 mW at 40 MSPS. The power-down feature on both products reduces power consumption to 15 mW.

The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

To ease interfacing to lower voltage systems, the digital output driver power pins of the ADC14L020/40 can be connected to a separate supply voltage in the range of 2.4V to the analog supply voltage.




### Features

- Single 3.3V supply operation
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Duty cycle stabilizer
- Internal reference
- Power-down mode

The ADC14L020/40 provide an impressive 74 dB SNR and 93 dB SFDR at Nyquist while consuming just 150 mW, making them ideal for portable medical imaging, instrumentation, home gateways, and communications receivers. These converters are available in LQFP-32 packages and operate over the industrial temperature range of -40°C to +85°C.

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BY MAURY WRIGHT, EDITOR IN CHIEF

# Slack EDA-market growth doesn't portend chip trends

A less-than-stellar record of recent growth in the EDA industry has been a hot topic. Clearly, such trends matter greatly to the companies that sell EDA tools. But, too often, observers relate tough times in the EDA market to potential softness in the semiconductor business. That link is tenuous at best. In fact, a recent DesignCon panel that set out to discuss stagnant EDA growth ended up pointing out just how big the separation between EDA and the semiconductor industry can be.

In a panel called "Why is EDA stagnating, or is it?" the group quickly agreed that the market was stagnant and even why that's so. Richard Tobias, vice president of engineering at Pixelworks, stated, "We need innovation in ESL [electronic-system level] and DFM [design for manufacturing]. The core place and route [segment] is stagnating."

Gary Smith, vice president and chief analyst at Gartner Dataquest, agreed. Smith pointed out that an increasing number of design engineers are now using tools developed in-house. Smith pegged the number of such users at 27%, whereas he claimed only about 10 to 12% of "power users" have relied on in-house tools in the past. Smith claimed that the trend is largely due to the lack of commercially available ESL tools. For more details centric to the EDA industry, check out the information in **Reference 1**.

Although I found the EDA-industry discussion interesting, I found the insights into the semiconductor market even more fascinating. Indeed, although ESL and DFM may enable innovations in semiconductors, the semiconductor industry drives EDA.

A couple of the panelists made statements about the chip business that both help explain the slow EDA segment and run counter to themes from the EDA crowd. Len Perham, chairman of Optimal, for instance, challenged the notion that ASIC-design starts will continue to decline. Perham basically questioned how we can have an explosion of compelling new consumer products while the chip industry designs fewer ICs. And, Perham was quick to warn that the bulk of the design activity may not be at the leading-edge process nodes. On the subject of process, he stated, "0.11 micron is going to have a very long life."

Tobias of Pixelworks made a similar point. He claimed that, even in instances in which a design team does an SOC (system on chip) in, say, a 90-nm process, support chips might use a trailing-edge 180-nm process.

I also believe that many designs will stay at 130-nm and less dense geometries (**Reference 2**). There is no question that PC processors, memory, FPGAs, and handset chips can benefit from the latest process. Most other designs would benefit from the less complex design issues at 130 nm and above. And I bet that this trend is having some effect on EDA growth. Design teams that stay at 130 nm and above don't need new tools.

Of course, the question remains concerning why analysts continue to report a drop in ASIC-design starts. I don't have an answer. But I've always wondered how EDA companies and analysts alike count the ASSPs (application-specific standard products) that fabless-semiconductor companies develop. Those designs rely on the same tools and travel through fabs in the same way as an ASIC that an OEM-design team develops. Does it count as an ASIC-design start when a merchant semiconductor company does an ASSP? I've yet to get consistent answers to that question.

Panelist Jim Hogan, general partner at Telos Venture Partners, did note, "There are a lot of design starts that aren't even measured." EDN

*Contact me at mgwright@edn.com.*

## REFERENCES

1. Mutschler, Ann Steffora "Help wanted: ES level evangelist to drive EDA growth," *Electronic News*, Feb 8, 2006, www.reed-electronics.com/electronicnews/article/CA6305703.html.
2. Wright, Maury, "Are cell-based ASICs going away?" *EDN*, Dec 5, 2005, pg 14, www.edn.com/article/CA6288036.

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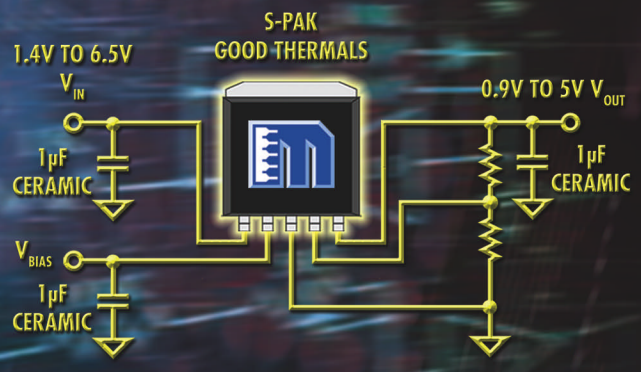


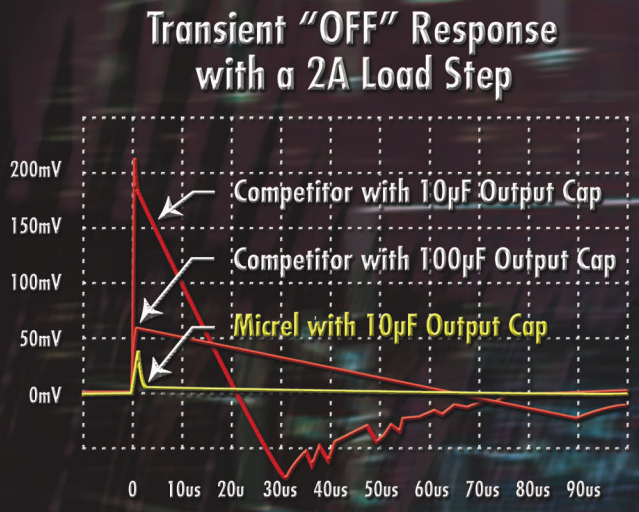


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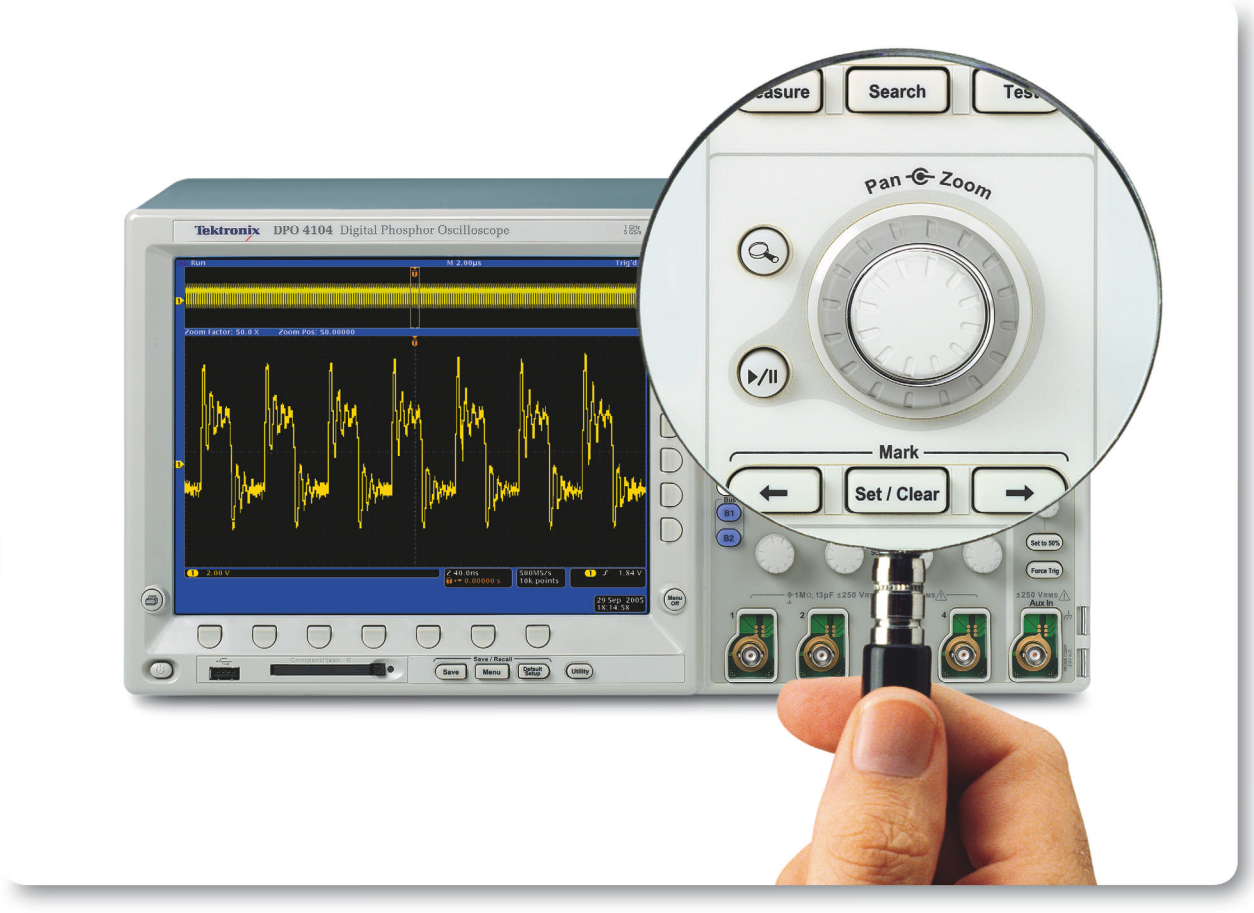


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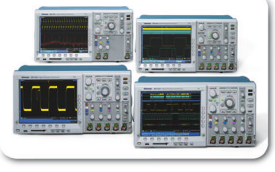

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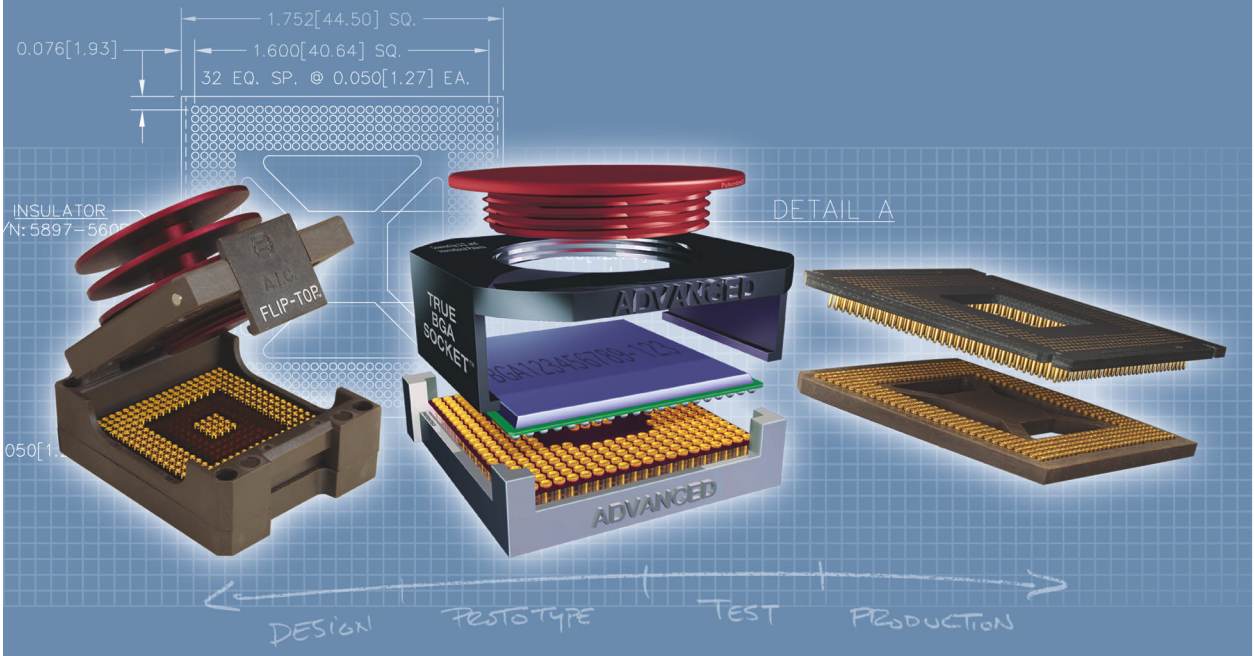


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# Ultracapacitor family targets minimal series resistance and cost

Ultracapacitors, also sometimes called supercapacitors or electric double-layer capacitors, have long offered promise in power applications alongside of and in place of batteries. The products can handle a million charge/discharge cycles and can provide a power boost for engine and motor starts in applications ranging from consumer electronics to hybrid vehicles. But cost has hampered the adoption of the technology. Last year, Maxwell Technologies introduced one ultracapacitor cell—the 2600F MC2600—that brought the price of the technology to 1 cent per farad. Now, the company is expanding the low-cost offering in cells ranging from 650 to 3000F and in modules that gang multiple cells.

The new members of the Boostcap family are cells and modules for either power or energy applications. Power applications include hybrid vehicles, distributed power systems, and others that demand the lowest possible series resistance. The energy line uses a lower cost electrode with higher series resistance and typically serves in roles such as battery backup or as a sporadic current boost in telecom systems to automatic meter-reading systems. The new family represents a better than halving of the cost of the earlier Boostcap family that the company announced four years ago.**—by Maury Wright**


Available both in individual cells and in multicell modules, the Boostcap family of ultracapacitors targets applications such as a motor-start power source in hybrid vehicles.

▷**Maxwell Technologies**, www.maxwell.com.

# Platform captures, processes, displays broadband data

Targeting transceiver applications, such as military radios and commercial wireless base stations, Pentek recently introduced the VME-based RTS 2502 development platform for real-time wideband-data acquisition, signal processing, and recording. The combination of data-recording and -playback capabilities in a single unit allows developers to capture and generate signals in real time for validation of signal-processing algorithms and system hardware.

Each 6U VME card in an RTS 2502 system accepts signals through two 14-bit ADCs operating as fast as 105 MHz and passes the signals through digital downconverters to Virtex-II FPGAs for signal processing and data handling. The unit can send raw or processed data to a disk array at speeds as high as 160 Mbytes/sec for recording, and the unit can also send the data off-board through an FPDP (front-panel data port), a Race++ port, or a Gigabit Ethernet port.

Pentek's RTS 2502 transceiver-development platform offers real-time, wideband-data recording and playback.

Two playback channels each offer digital upconversion and dual 500-MHz, 16-bit DACs to produce either real or I/Q RF signals, drawing data from other I/O or the disk array at speeds as high as 160 Mbytes/sec.

Pentek's GateFlow FPGA-design kit includes design information, software files, optimized DSP functions, and development utilities. The company's SystemFlow software includes API (application-programming-interface) libraries for the target board, as well as control libraries for the host PC. The software package also includes a data viewer, written in LabView, that displays collected data in either the time or the frequency domain. Prices for the RTS 2502 system start at $29,995 for hardware only and $41,495 with bundled SystemFlow and GateFlow software.**—by Warren Webb**

▷**Pentek Inc**, www.pentek.com.

# Cores lower entry cost for custom SOCs

Tensilica based its new Diamond Standard family of processor configurations on the Xtensa architecture. Each core implements the Xtensa instruction-set architecture in a five-stage-pipeline, 32-bit architecture. The cores support modeless switching between 16- and 24-bit instructions to deliver high code density, high processing performance, and low power consumption. These processors offer a lower price to design teams considering the Tensilica technology. The company's Diamond Standard family includes six processor configurations.

The family comprises the 108Mini, a cacheless RISC-controller processor, which delivers lower power consumption than ARM7-based approaches. The smallest device in the family, the 108Mini uses a 0.38-mm$^2$ cell area in a 0.13-micron process and consumes 0.06 mW/MHz with the 0.13LV libraries or 0.09-mW/MHz with the 0.13G libraries.

The low-power, 24-bit Diamond 330HiFi audio processor supports audio and speech codecs; Tensilica based it on the Xtensa HiFi 2 audio engine. It supports decoding and encoding for Dolby Digital AC-3, MP3, aacPlus, and WMA; SBR (spectral-band replication); parametric stereo; QSound MIDI; 3-D audio; and G723-1 and G729AB VOIP (voice-over-Internet Protocol) codecs. The midrange Diamond 212GP RISC controller offers DSP support, including 16 MACs (multiply/accumulates), 16 multipliers, minimum/maximum operations, clamps, sign extend, and NSA instructions. It includes instruction and data caches, as well as user-selectable local-memory sizes, and it competes with ARM9-based approaches for better processing performance and lower power consumption. It uses a 0.58-mm$^2$ cell area in a 0.13-micron process and consumes 0.085 mW/MHz with the 0.13LV libraries or 0.135 mW/MHz with the 0.13G libraries.

The midrange Diamond 232L RISC-processor core includes a full MMU (memory-management unit) to support the requirements of the Linux operating system. It includes the same DSP support as the 212GP. The core requires a 0.71-mm$^2$ cell area in a 0.13-micron process and consumes 0.10 mW/MHz with the 0.13LV libraries or 0.145 mW/MHz with the 0.13G libraries.

The high-performance, three-issue Diamond 570T static superscalar processor core competes with the ARM1136JF-S core based on EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) benchmarks. The core includes both a 32-bit input and a 32-bit output queue that support direct access to data from the pipeline with no loads or stores. The core uses a 0.96-mm$^2$ cell area in a 0.13-micron process and consumes 0.11 mW/MHz with the 0.13LV libraries or 0.15 mW/MHz with the 0.13G libraries. The highest performance Diamond 545CK licensable core delivers digital-signal processing using a three-issue VLIW (very-long-instruction-word) processor containing eight MACs that support SIMD (single-instruction-multiple-data) operations. The core includes a Viterbi accelerator to support communications baseband applications.

The price for the Diamond 108Mini is $75,000 for a single-use license with a royalty fee of 5 cents per core. Tensilica's XCC optimizing compiler and Eclipse-based Xplorer IDE support software development on these processors with a clock-cycle-accurate, pipeline-modeled instruction-set simulator; a Gnu-based tool chain, including an assembler, a debugger, a profiler, and a linker; and optimized C libraries. Operating-system support for these cores includes Accelerated Technology's (www.acceleratedtechnology.com) Nucleus Plus, micro-Itron from Sophia Systems (www.sophia.com), Tensilica's runtime XT-OS, and open-source eCOS. Linux support for the Diamond Standard 232L is available from MontaVista's (www.mvista.com) Linux Professional.

**—by Robert Cravotta**

▷**Tensilica**, www.tensilica.com.

## FROM THE VAULT

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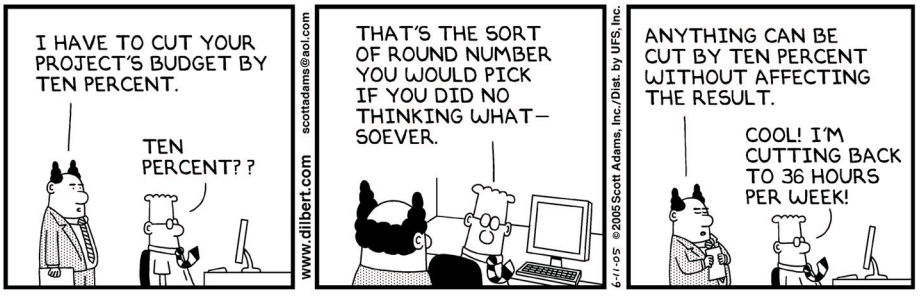
Jeff Montgomery, president, Gnostic Concepts, *EDN*, Oct 14, 1981

**DILBERT** *By Scott Adams*



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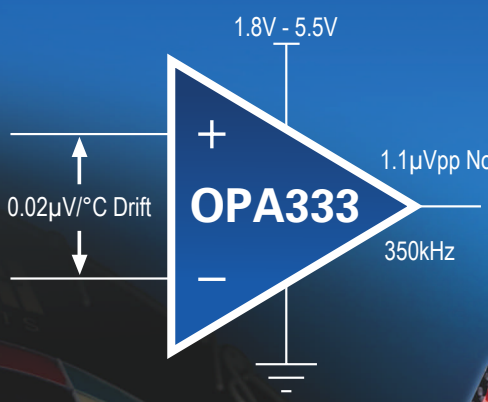


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# Sigma-C and Mentor make strides in DFM

Announcements from Sigma-C and Mentor Graphics bode well for IC-design groups wanting to spot and fix lithography hot spots in their IC layouts before they send their designs to the mask shop. Sigma-C has announced the Solid+ microlithography simulator for design and OPC (optical-proximity correction).

Meanwhile, Mentor Graphics' Calibre group has introduced a tool for mask makers. However, the company says that the product's underlying pixel-based simulation engine sets the stage for a bigger release, this year, of a design-centric microlithography simulator. The microlithography-simulation niche of the DFM (design-for-manufacturing) market is becoming important as process geometries shrink below 90 nm, driving mask costs into the millions of dollars. Masks on these processes require OPC on all layers and thus take more effort and cost.

With Solid+, engineers use full-chip, third-party lithography simulators to locate trouble spots and then use Solid+ to do detailed 3-D analysis, says Peter Feist, chief executive officer of Sigma-C. Users feed Solid+ a GDSII file, and, after simulation, the tool generates a resist profile. Engineers can then overlay their desired layout and the simulated print showing how it would appear in the photo resist, thus exposing areas in which violations are likely to occur. The company has thus far identified three usage models for the tool.

First, IC and custom-cell designers can use the tool to perform resist-level simulation of layout and cells larger than 20×20 microns to let designers know whether the photo resist can accurately produce their patterns at smaller process nodes. Second, engineers can use the tool for developing OPC rules decks. Mask problems often occur because OPC rules are not well-defined; vendors build them using results from less-accurate 2-D simulators. Designers can use Solid+ to ensure the accuracy of OPC rules decks.

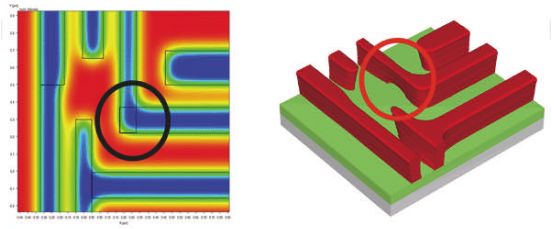
Mentor Graphics' OPC verification tool, OPCverify, mainly targets mask makers and qualifiers who want to check pattern fidelity before committing to a mask. The tool takes in the drawn layer, an OPC-corrected layer, and a run file and then uses a new pixel-based engine to simulate a silicon image as it would show up on the output of a scanner. The tool then gives a contour of every shape on the chip.

OPC engineers can also use the tool to ensure OPC rules are robust on many designs. OPCverify sets the stage for an upcoming release targeting IC designers. Lithographic simulation will become commonplace, but, to make it effective, designs have to take OPC into account—essentially imitating everything a fab facility does. "As we get to 65 and 45 nm, pattern fidelity is a huge issue," says Charlie Albertalli, product manager for Mentor. "It is getting harder and harder with low-k processes to absolutely replicate a design shape. Certain topologies look good at nominal dosage and focus, but, as soon as you remove the OPC, the image rapidly falls apart."

**—by Michael Santarini**

▷**Sigma-C**, www.sigma-c.com.

▷**Mentor Graphics**, www.mentor.com.



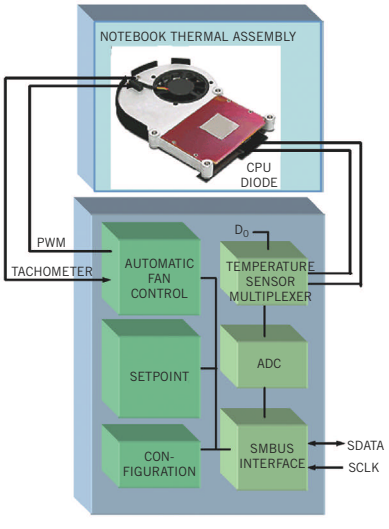
Sigma-C's Solid+ locates trouble spots (left) and then performs detailed 3-D analysis (right).

# Thermal escalation drives need for controlled active cooling

Thermal issues continue to escalate in the PC-processor sector. Early processors required huge passive heat sinks and then fans dedicated to the processor-cooling task. Now, reliable systems need active monitoring of systems and even chip temperature with real-time fan control. Andigilog targets just such applications with its ThermalEdge technology. The company has just announced two thermal-management chips: the aSC7512, which targets traditional motherboard designs, and the aMC8500 for the new BTX (Balance Technology Extended) technology. Intel (www.intel.com) designed BTX for shrinking form factors, and it moves the PC to mechanically separate subsystems with different cooling, power, and other needs.

The aSC7512 includes an on-chip temperature sensor and remote die-temperature-sensing capability using a connection to the diode integrated on a processor die. The chip supports three- and four-wire fans and integrates a digital filter that makes for smoother fan operation. The aMC8500 can drive a 1A, brushless-dc fan and integrates the requisite MOSFET motor drives. Andigilog will ship samples of the chips, as well as reference designs, in April. The aSC7512 will sell for $1.50 (1000), and the aMC8500 will sell for $1.45 (1000).**—by Maury Wright**

▷**Andigilog**, www.andigilog.com.




Connecting to an on-chip diode, the aSC7512 thermal-management chip takes real-time die-temperature readings and offers dynamic cooling-fan control.

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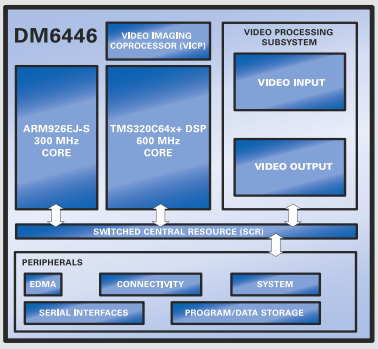
- TMS320DM6446 – Video encode/decode
- TMS320DM6443 – Video decode




### Performance Benchmarks:

| STANDALONE CODECS | DM6446 | DM6443 |
|---|---|---|
| MPEG-2 MP ML Decode | 1080i+ (60 fields /30 frames) | 720p+ |
| MPEG-2 MP ML Encode | D1+ | n/a |
| MPEG-4 SP Decode | 720p+ | 720p+ |
| MPEG-4 SP Encode | 720p+ | n/a |
| VC1/WMV 9 Decode | 720p+ | 720p+ |
| VC1/WMV 9 Encode | D1+ | n/a |
| H.264 (Baseline) Decode | D1+ | D1+ |
| H.264 (Baseline) Encode | D1+ | n/a |
| H.264 (Main Profile) Decode | D1+ | D1+ |

+ denotes available processor headroom for analytics and/or other features

### Tools: Validated Software and Hardware Development

- DVEVM (Digital Video Evaluation Module)
- MontaVista Development Tools
- Code Composer Studio IDE

### Software: Open, Optimized and Production Tested

- Platform Support Package
- MontaVista Linux Support Package
- Industry-recognized APIs
- Multimedia frameworks
- Platform-optimized, multimedia codecs:
  - H.264
  - MPEG4
  - H.263
  - MPEG2
  - JPEG
  - AAC+
  - AAC
  - WMA9
  - MP3
  - G.711
  - G.728
  - G.723.1
  - G.729ab
  - WMV9/ VC1

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## Round table mulls hard-IP-at-board-level concept

Sometimes, a panel discussion ends up more like a round table. That scenario happened at DesignCon in February, with a panel that design consultant Pallab Chatterjee organized on hard IP (intellectual property) and whether it can exist for board-level designs. At the chip level, "hard IP" refers to a block of circuitry that a designer has verified, placed, and routed, so that you can drop it into a chip design intact during the physical-design process. In some cases, you can insert hard IP into the design at the foundry just before mask creation.

Can a similar concept exist for board-level design? Chatterjee opened the discussion, observing that some board-level reference designs go all the way to specifying components and providing Gerber files for creating board film. But then he pointed to several examples of designs in which the form factor of the final product makes it impossible to use the reference design without significant modification, and this modification invalidates the electrical verification designers perform on the reference design.

The panelists included Chatterjee; Vipul Badoni, senior manager of the high-speed-I/O-Applications-engineering group at Altera; Jerry Durand, chief executive officer of Durand Interstellar; and John Isaac, director of market development for the systems-design division at Mentor Graphics.

**What comes with an Altera reference board?**

**A** Badoni: "If you purchase one of our reference designs, you get a full [Cadence] Allegro database with constraints, schematics, and documentation with design guidelines. We even give you the guidelines we gave to the pc-board designer to design our board.

Isaac: One of the most important things chip vendors deliver to customers are models. Any customer today that takes a reference design as a drop-in core, slaps it in their design, adds a little logic, and intends to make 100 of them is crazy. The performance of signal-integrity models that vendors supply is important.

**How much information do you have to model that is in the reference design that may not be just datasheet specs of the FPGA? Do you provide signal-integrity models for the traces that connect the reference design to the outside world?**

**A** Badoni: Yes. We work with vendors to get connection models in with our reference designs. In modeling, if you get garbage in, you get garbage out, so you have to be careful with what you supply. Don't substitute a Micron DIMM for an Infineon DIMM and expect it to work. You have to secure the right models to make sure they work.

**What are the worst problems designers face today?**

**A** Badoni: The most prevalent problem we are dealing with today is power delivery.

Durand: It's a problem because of built-in contradictions. For instance, the power-delivery specs on complex chips often say the parts are supposed to have low impedance to the power and ground planes. But if that chip is in a MicroBGA package, you are using 6-mil laser-drilled vias that go down only 0.005 in., or one layer. So, it gets hard to have super low impedance to power and ground planes that are 0.020 in. below the via.

Badoni: Monitoring the power-delivery systems is also tough because you have to model passives in Spice, which is not inherently a passive-modeling technology. You have to figure out what capacitors you can put in your system.

> "Any customer today that takes a reference design as a drop-in core, slaps it in their design, adds a little logic, and intends to make 100 of them is crazy.

Durand: Power is a big problem, especially in MicroBGA packages in which a single device can have a mix of pins with different voltages. Layout is difficult with alternating 2.5, 1.8, and 3.3V pins. You can't even run a heavy bus up to catch those pins. If you had four in a row, you could drill a via to connect them, but if you intersperse them, you wind up with fine traces running your power into the lead; it is the only physical way to do it.

**Who owns SIP (system-in-package) design: IC designers, pc-board designers, or a separate group?**

**A** Chatterjee: Speaking from the chip-design world, I don't know anyone who would willingly want to take on that set of problems.

Isaac: One of the advantages of SIPs is that a lot of the parts are off-the-shelf. You may design an IC to put in a SIP and then grab parts from other people and add some discretes. It soon becomes a cross between IC and pc-board design.

**–by Ron Wilson and Michael Santarini**

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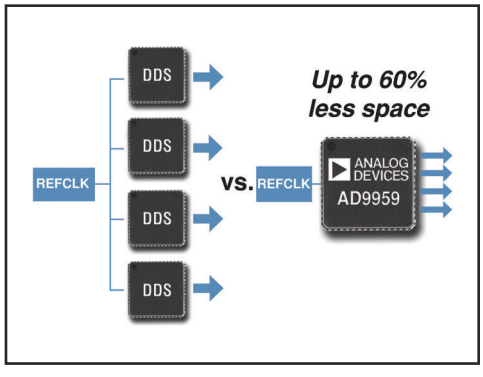


*Old multichip solution vs. new quad DDS.*

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# Korea gets WiMax certification lab

Momentum for WiMax (Worldwide Interoperability for Microwave Access) wireless-broadband technology continues to build—especially outside North America. Korea is an early adopter of wireless services and is leading the WiMax charge with a new certification lab. To handle the expected deluge of WiMax gear, the WiMax Forum chose Spain's Cetecom Laboratories (www.cetecom.es) as the first laboratory and recently added Seoul, South Korea's TTA (Telecommunications Technology Association www.tta.or.kr) as the second.

TTA will likely specialize in certification of products that conform to the coming mobile flavor of WiMax, IEEE 802.16e. South Korea is launching WiBro (wireless-broadband) technology that is essentially the basis for mobile WiMax. TTA plans to have the WiMax lab operating by the second quarter of this year. It expects to certify the first commercial mobile-WiMax product in the first quarter of 2007.

In other WiMax developments, Cetecom Laboratories is also preparing to offer mobile-WiMax certification. The lab is jointly developing a protocol-conformance tester with Aeroflex (www.aeroflex.com). Cetecom and UK-based picoChip (www.picochip.com) have just announced that the tester would rely on the PC102 DSP-array chips and the PC8530 software stack from picoChip. Cetecom hopes to begin mobile-WiMax testing by the end of the year.

**—by Maury Wright**

▷**WiMax Forum**, www.wimaxforum.org.

## SOC HOUSE PARTNERS WITH MALAYSIAN FAB

Belgium company Essensium, a provider of SOC (system-on-chip)- and ASIC-design services, recently received a significant boost with a funding infusion from investment company Atlantic Quantum, which Khazanah National (www.khazanah.com.my) owns. Khazanah also owns foundry Silterra (www.silterra.com). The €6 million investment will allow Essensium, a spin-off of IMEC (www.imec.be), to become an independent company, although it has access to IMEC's wireless, SOC, and system-in-package intellectual property.

**—by Maury Wright**

▷**Essensium**, www.essensium.com.

## SOM concept adds versatility to embedded computing

According to Advantech, SOM (system-on-module) computing is set to grow rapidly this year as more companies adopt the concept. The company sees SOM as a good fit for applications that have product volumes of 1000 to 10,000 units. At less than that level, a conventional single-board-computing approach is the preferred option; at high volumes, a custom design becomes more economic.

In the 1000- to 10,000-unit range, Advantech designs a target board for the application. The board contains the functions that the task requires in addition to the basic computing capability. It then provides the computing power in the SOM, which plugs into the system board. This approach provides advanced computing power in an easy-to-use format, because the critical parts of the design—those close to the CPU itself—exist in a fully developed, stable condition. Users also have the option of changing or upgrading processors by replacing the module.

Advantech's SOM-device support includes Com Express, ETX, PCI-bus SOM-144, and the company's A200 series of modules. Advantech based the A2200 RISC platforms on PXA and other ARM9 chips for mobile and low-power applications. Advantech states that, although recent coverage associates the SOM concept with newer, high-power processors, it can host any level of CPU from 486 to Pentium M or Xeon chips. The company aims to provide a complete design package, interpreting the "platform" as hardware, software, and any required design services. Distributed design centers can access Advantech's corporate IP (intellectual-property) resources, and the company's in-house prototyping production line can produce sample lots of as many as 30 pieces of a board design, with a target time of two months from design start to delivery.

Advantech is working on a modular-I/O concept to match the processor boards with preconfigured modules for applications that require connectivity exceeding that of the standard modules.

**—by Graham Prophet, *EDN Europe***

▷**Advantech**, www.advantech.com.

## Oscillator pushes to 192 GHz for detection applications

03.16.06

Taiwan-based UMC claims to have produced the highest frequency VCO (voltage-controlled oscillator) yet to be fabricated in silicon. The University of Florida's Department of Electrical and Computer Engineering (Gainesville, FL, www.ece.ufl.edu) designed the VCO, which operates at 192 GHz. UMC officials believe that designers can use the VCO in a variety of sensitive detection applications, such as chemical detection, detection through fabric, imaging through fog and clouds, and even the detection of skin cancer.

UMC built the VCO using its 130-nm RF-CMOS process. The device has a "push-push" design, meaning that the output frequency is only double the core frequency, whereas some VCOs multiply the core frequency by three or four, resulting in relatively weak output. UMC's VCO provides —20 dBm and consumes 11 mA from a 1.5V supply.—by Maury Wright

▶**UMC**, www.umc.com.

LEADING inside

A series of engineering insights
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# The Importance of Differential Measurement

Many real world applications require amplifying a very small signal in a high noise environment. Usually, the signal sensor is located some distance from the amplifier. As a consequence, a large amount of noise and hum is often introduced.

Effective signal recovery often depends on carefully choosing the optimum amplifier for a particular application. There are three common types of systems in use: single-ended input and output (operational amplifier based), differential input, single-ended output (instrumentation amplifier based), and differential input and differential output (differential amplifier based) systems. Some designers may be tempted to use a single-ended, shielded cable system, similar to that shown in Figure A.

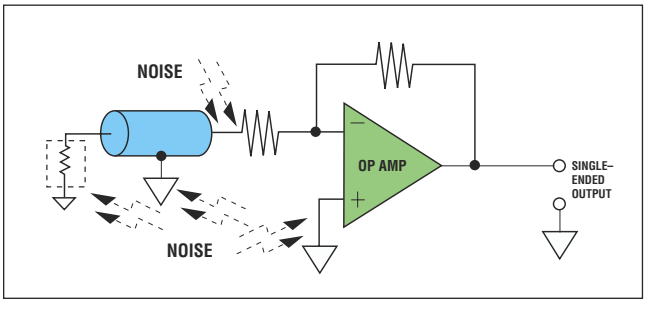


*Figure A. A single-ended measurement system*

Here, the input is applied between the shielded cable and common or "ground," then travels through the cable to the op amp. A single-ended system like this is very prone to noise pickup because the signal is referenced to ground, i.e., the signal flows through the system ground, with noise being added along the way. With a single-ended system like this, both the signal and the noise are amplified. The common practice of removing the noise at the amplifier output, using low-pass, high-pass, or band-pass filtering, is often ineffective. In some cases, the total noise can be much greater than the signal itself.

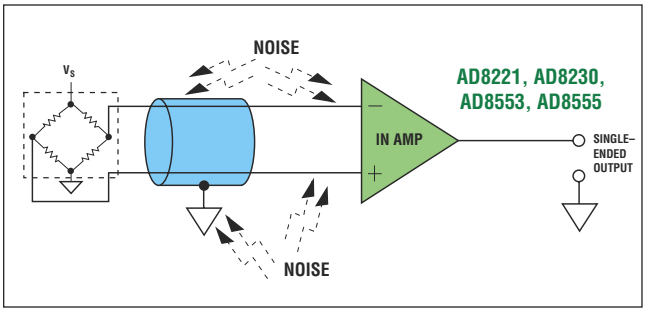


*Figure B. A differential input, single-ended output measurement system*

Figure B shows a better method for recovering weak signals. Here, the input signal source is differential. Simply stated, this means that the signal is applied *between* two input lines, with *no* signal traveling through the ground connection. This type of system normally uses an in-amp which has a differential input and a single-ended output. Much of the noise that is the same (common mode) on both lines is rejected by the in-amp, which only amplifies the differential input signal.

Note that the inputs of most instrumentation amplifiers require a dc return path (using resistors, for example) for the amplifier's input bias currents. This is very important for ac-coupled, single-supply applications where it is also often necessary to have the amplifier's input common-mode reference and output reference raised above ground.

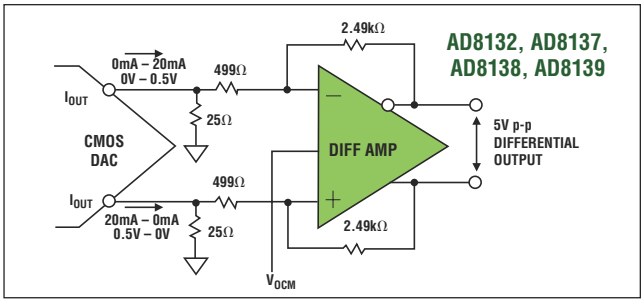


*Figure C. A differential input, differential output amplifier used as a high-speed DAC buffer*

Figure C is a system featuring an amplifier that has both a differential input and output. These are commonly used in high bandwidth applications, such as driving ADCs or buffering DACs.

For more information on using operational amplifiers, instrumentation amplifiers, differential amplifiers, and other signal processing components, please visit *www.analog.com*.

In addition, you can view these following online seminars: "Looking at the World Different(ial)ly" and "In-Amps: Common Applications Problems and Solutions" both at: *www.analog.com/onlineseminars*.

Finally, you can download or receive a hard copy of the design handbook "A Designer's Guide to Instrumentation Amplifiers, 2nd Edition" at *www.analog.com/inampguide*.

*Author Profile:* ***Chuck Kitchin*** *has been a hardware applications engineer with Analog Devices for 29 years. In addition to developing new circuits, he has published three books and close to 100 technical articles.*

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| Si530 | Dual XO | | | | | |
| Si534 | Quad XO | | | | | |
| Si550 | VCXO | ±20 ±50 ±100 | 10 MHz–1.4 GHz | LVPECL LVDS CML CMOS | 5x7mm | 3.3 V 2.5 V 1.8 V |
| Si552 | Dual VCXO | | | | | |
| Si554 | Quad VCXO | | | | | |

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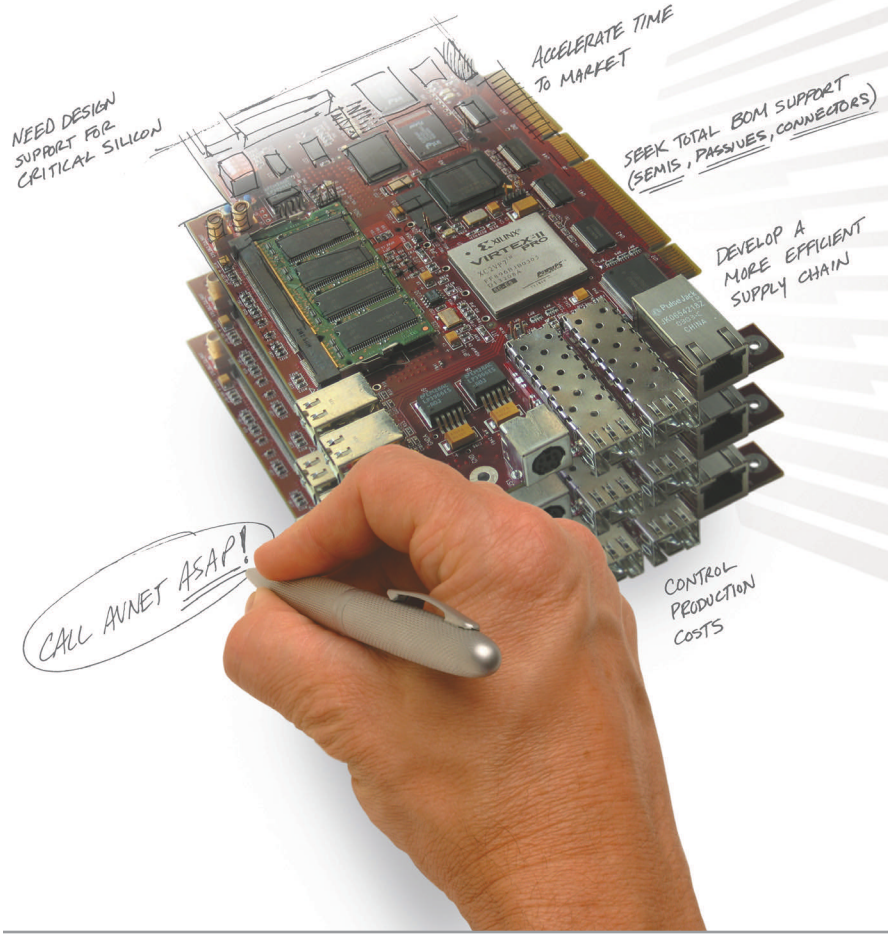


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BY BONNIE BAKER

# Choosing SAR versus high-speed delta-sigma ADCs

Delta-sigma-ADC technology has caught up to that of SAR (successive-approximation-register) ADCs in sampling frequency. A crossover in the sampling-time regions of approximately 100 kHz to 1 MHz exists in both types of devices. These two types of converters also match in most key specifications. For instance, are you concerned about the dc characteristics of offset voltage and gain error, or are you more concerned about the ac specifications, such as noise or THD (total harmonicdistortion)? You may find SAR and high-speed delta-sigma converters that have equivalent specifications in the dc realm, as well as the ac specifications.

So which device do you choose for your application circuit? To make that determination, you need to compare the operation of these two devices. A/D-conversion latency is the time the ADC takes to go from one sample to the next, including the data-retrieval time. SAR-converter latency comprises a "snapshot" of the signal and the serial retrieval of the data. In contrast, the delta-sigma ADC has a larger output-code delay because the converted signal does not correspond to a single point in time. The delta-sigma converter quickly averages the input for a predetermined time before outputting the digital code at higher speeds (**Figure 1**). The trade-off between the converters is that the delta-sigma ADC consumes more power due to higher clock rates.

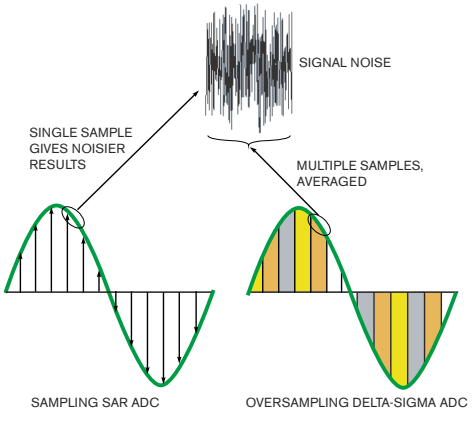


Figure 1 A SAR converter takes several "snapshots," capturing the waveform. The delta-sigma ADC averages during the sample period, providing signal filtering.

A common disappointment when you use a SAR converter is the presence of large variance in the output code for a dc input signal. The problem often is not the converter, but how you implement the application circuit. A SAR converter has a wide input bandwidth and fast reaction to signal changes. The one-time-sample-per-conversion architecture effectively captures the signal and its noise. This type of converter in a noisy environment requires a high-order, antialiasing filter. The addition of an antialiasing filter solves the noise problem but increases the settling time of the converter system. The system settling time is an issue in multiplexed-system applications.

In contrast, a delta-sigma converter averages multiple samples at a higher data rate for each conversion result. The digital filter in these converters acts as an antialiasing filter, so that the converters need only an external second-order lowpass filter on the analog input. A delta-sigma converter easily handles signal noise with its internal digital-filtering system. However, if you present a step input to the delta-sigma-converter input, the converter also requires time to settle. The on-chip digital filter requires time to refill and resettle.

Both types of converters offer other benefits. SAR converters can have embedded multiplexers or PGAs (programmable-gain amplifiers) at their inputs. Some delta-sigma converters have multiplexers and PGAs, but they may also have input buffers, sensor-burnout current sources, and higher order systems than do SAR converters. On the application level, how do you differentiate between these converters? SAR converters suit applications that require fast response and low latency, such as high-speed control loops and multichannel data-acquisition systems. Delta-sigma converters target applications that require high resolution, such as scales or audio systems. However, both types of converters find use in motor control, sonar, and vibration analysis, which require precision, wide bandwidth, and high-resolution operation. EDN

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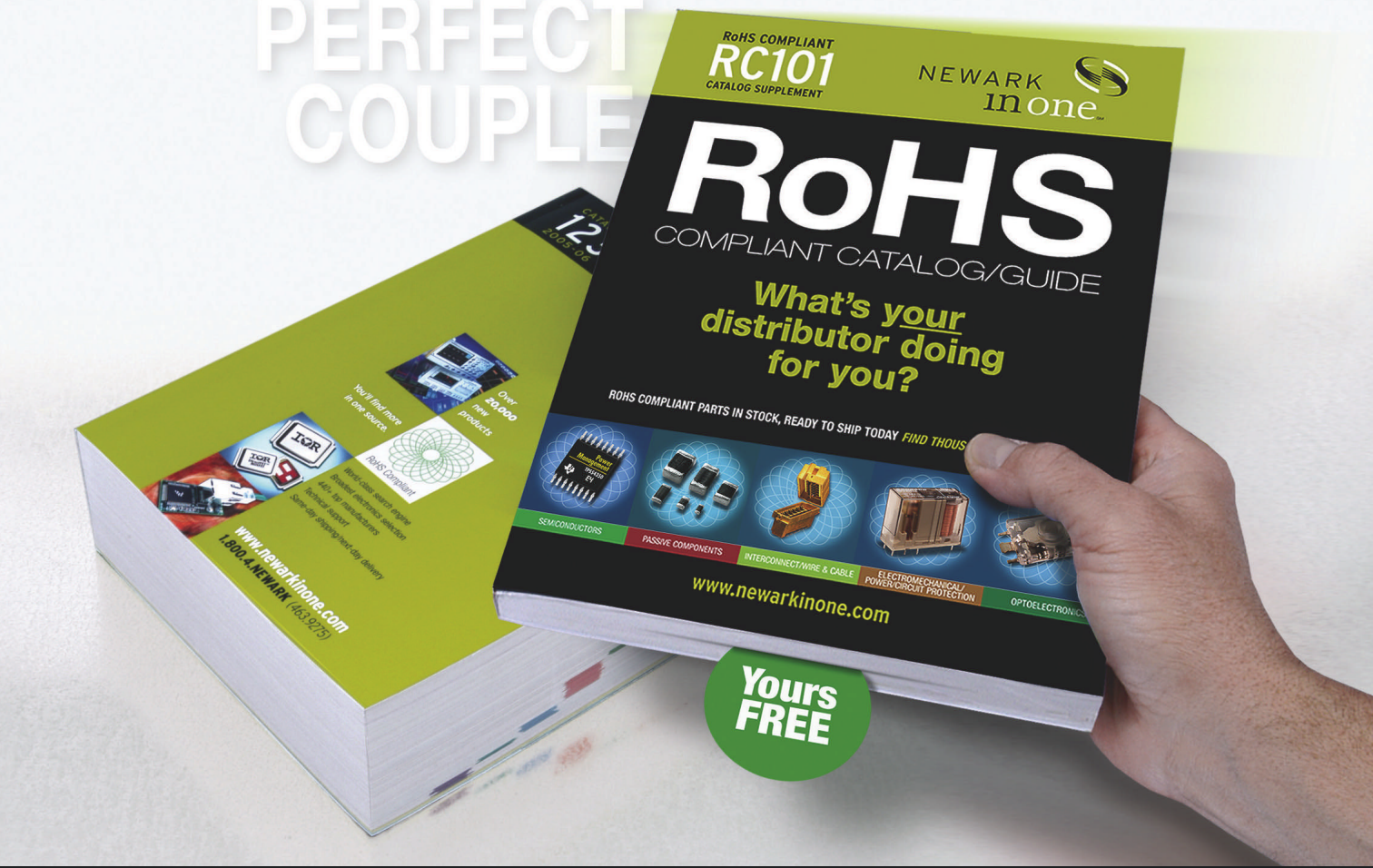
*Bonnie Baker is the author of* A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

# THE PERFECT COUPLE

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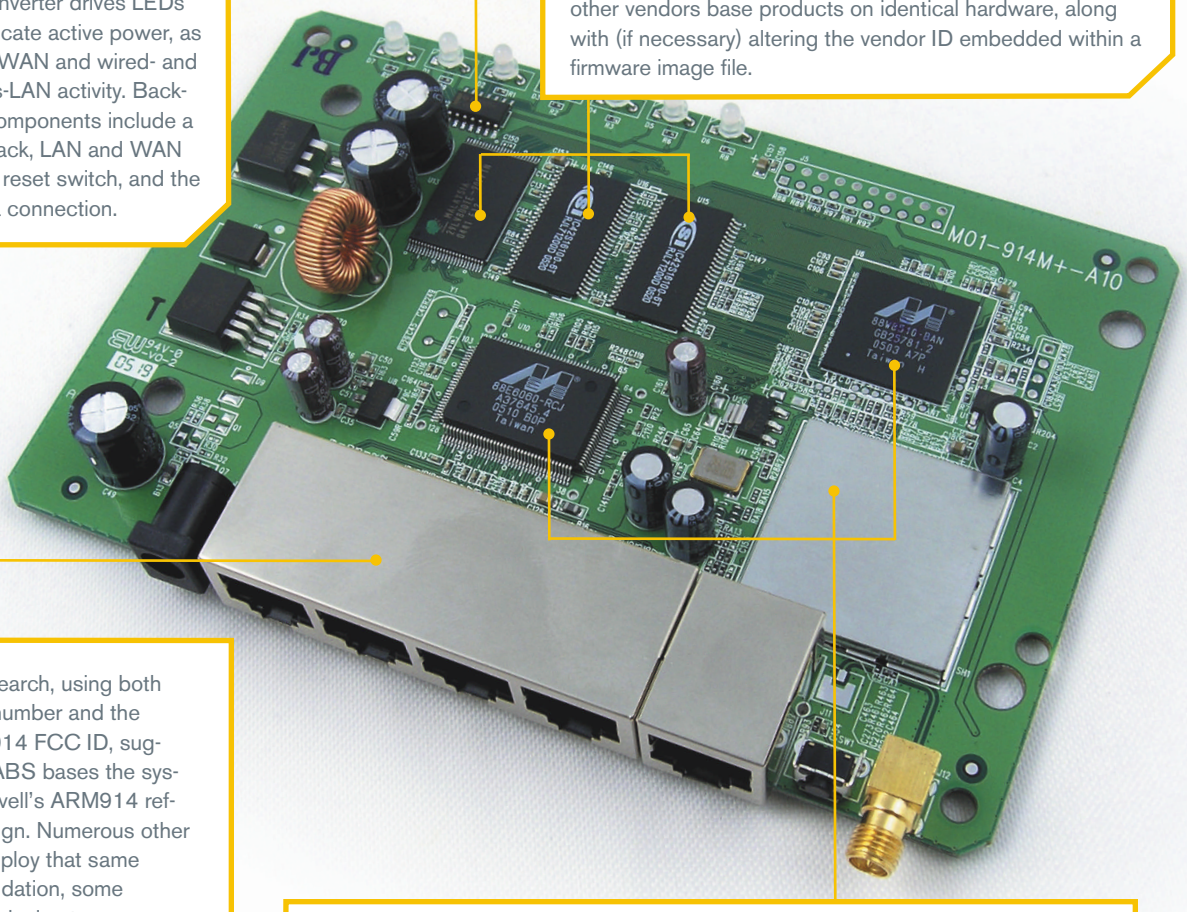
- Go to www.edn.com/article/CA6305354 to see last month's USB-audio-peripheral teardown.

# Figuring out the no-cost route

Last month, *EDN* dissected a $20-on-clearance (previously $50) USB audio peripheral. This month, we continue our fiscally focused analysis with ABS's NW-203-RT $0-after-rebate 802.11g- and four-port switch-inclusive router. What's inside the purple-tinted plastic, and is ABS turning a profit at $20?

A Texas Instruments SN74LVC14 hex Schmitt-trigger inverter drives LEDs that indicate active power, as well as WAN and wired- and wireless-LAN activity. Back-panel components include a power jack, LAN and WAN ports, a reset switch, and the antenna connection.

The memory subsystem includes an 8-Mbit, 90-nsec Fujitsu 29LV800 flash memory with a hardware-selectable 8- or 16-bit data bus and its hardware-lockable boot block at the top of its memory map. It also employs two Winbond W981616-BH 16-Mbit SDRAMs with 16-bit data buses. Enterprising hackers have been able to correct some of the router's DHCP (Dynamic Host Configuration Protocol) and DNS (domain-name-serve) functional glitches, as well as add features, such as WPA2 (Wi-Fi Protected Access 2) support. They've accomplished these feats by figuring out which other vendors base products on identical hardware, along with (if necessary) altering the vendor ID embedded within a firmware image file.




Internet research, using both the model number and the MQ4ARM914 FCC ID, suggests that ABS bases the system on Marvell's ARM914 reference design. Numerous other vendors employ that same design foundation, some choosing a dual-antenna configuration. Visit the discussion thread at www.dslreports.com/forum/remark,10883070 for more details.

Marvell's Libertas chip set comprises the 88W8000 RF transceiver under an EMI-suppressing Faraday cage; 88W8510 ARM-based SOC (system on chip); and 88E6060 six-port switch, of which the NW-203-RT implements only four LAN ports. The pc board contains signal traces on both sides, along with embedded power and ground planes. The backside of the pc board, not shown, contains no circuitry, only through-hole solder points, test points, and traces.

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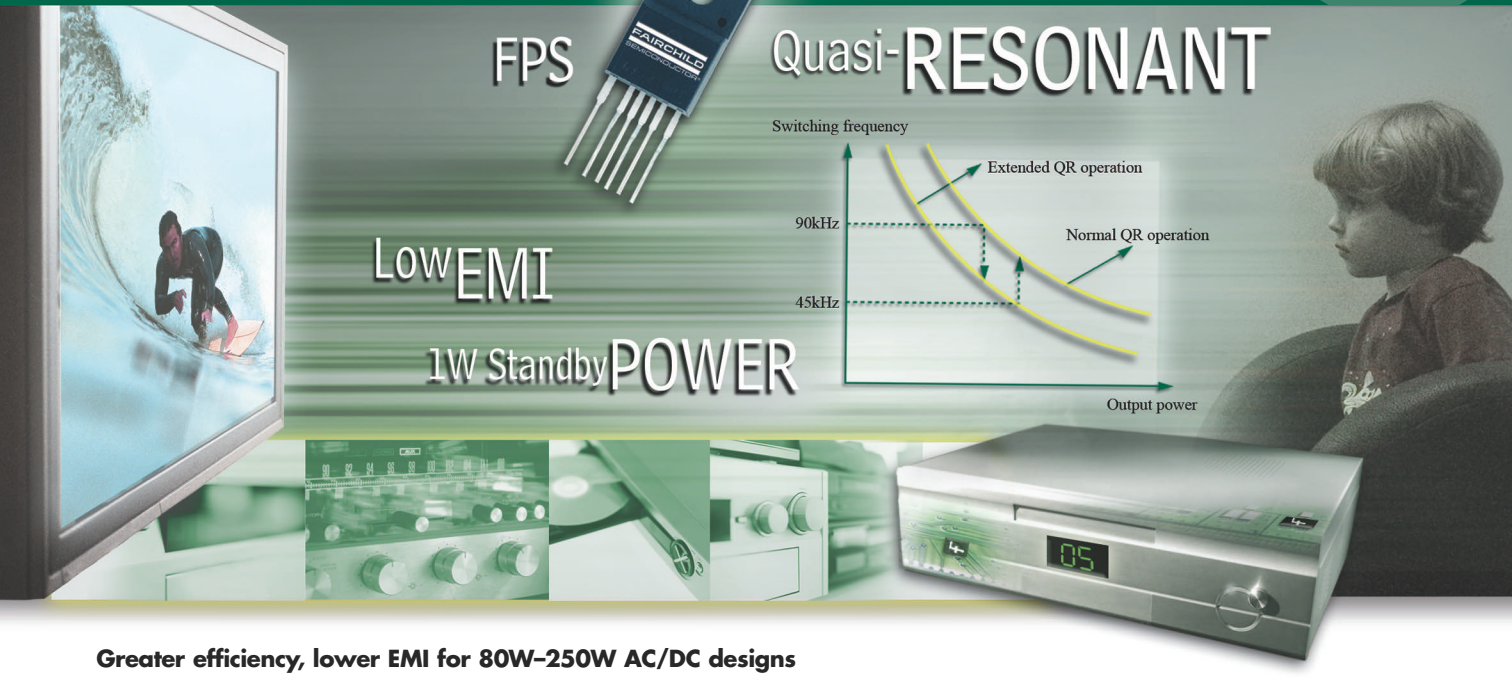


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| FSCQ1465RT | 160 | 8 | 0.8 |
| FSCQ1565RT | 170 | 8 | 0.7 |
| FSCQ1565RP | 210 | 11.5 | 0.7 |

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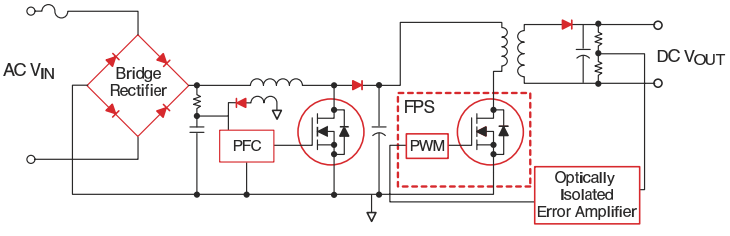


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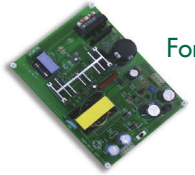

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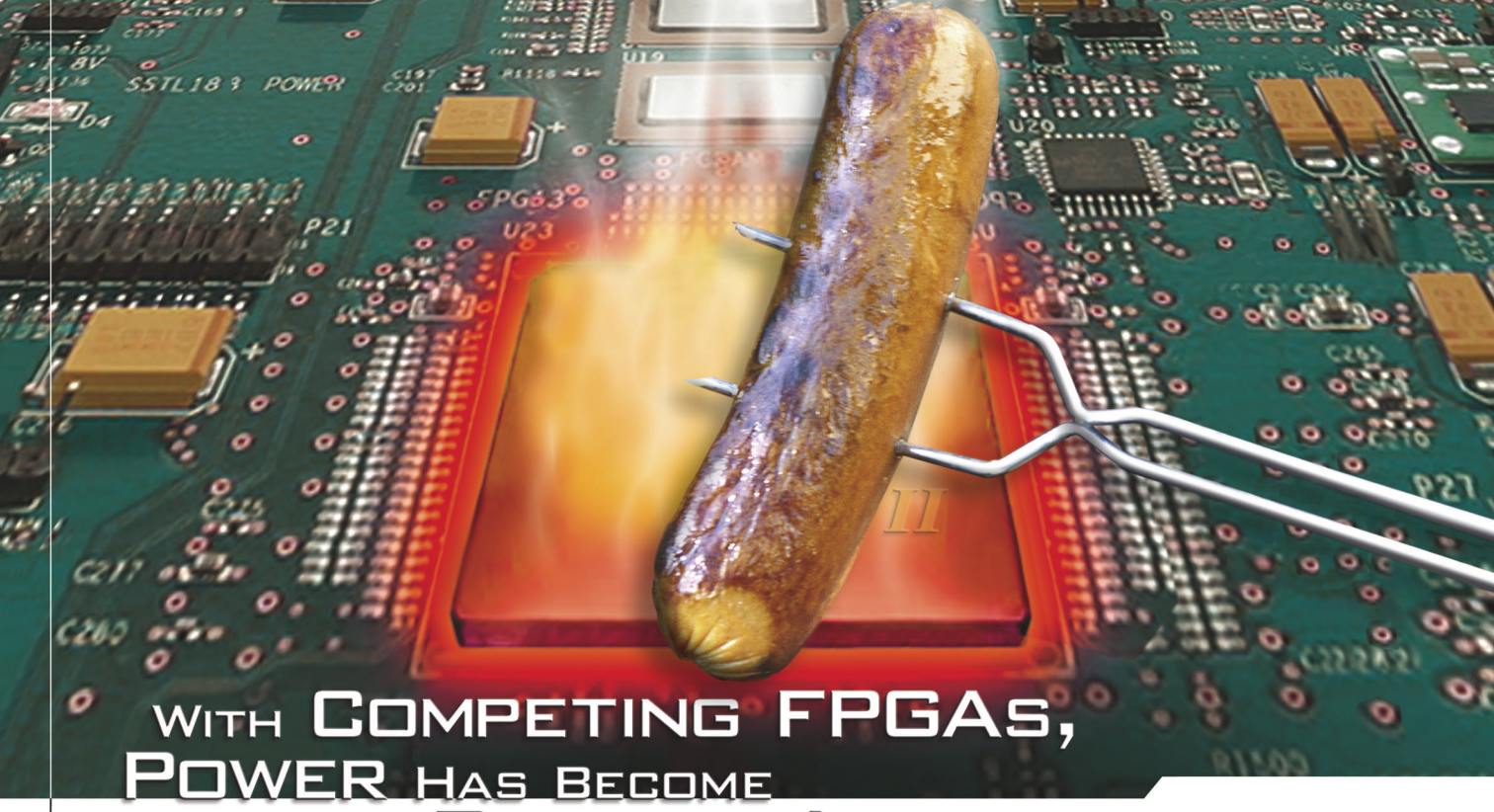

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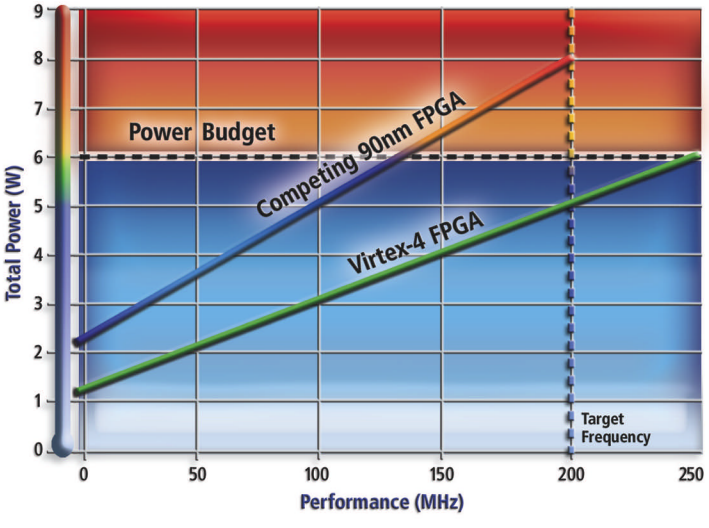


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BY RICHARD A QUINNELL • CONTRIBUTING TECHNICAL EDITOR

# ROHS compliance: IT'S NOT EASY BEING GREEN

EUROPEAN ENVIRONMENTAL DIRECTIVES TAKE EFFECT SOON, LEAVING MANY US COMPANIES STRUGGLING TO OVERCOME THE CHALLENGES OF IMPLEMENTING COMPLIANT DESIGNS.

On July 1, 2006, electronic equipment sold in the European Union will have to comply with the ROHS (reduction-of-hazardous-substances) directive or face both removal from the market and assessment of substantial fines. However, some exemptions to this act are causing component suppliers to offer both ROHS-compliant and -noncompliant stock. This situation leaves design engineers with the sometimes-frustrating task of finding and qualifying the right components to ensure a compliant product.

The ROHS directive seeks to prevent environmental damage by eliminating dangerous materials from electronic equipment that may eventually find their way into landfills where they can contaminate ground water (see **sidebar** "ROHS in brief"). To enforce compliance, the directive allows member states to ban the sale of noncompliant products and to levy substantial fines on the product manufacturers. Manufacturers that fail to adhere to the ROHS directive thus risk losing out on participation in a multibillion-dollar market with some 400 million potential customers.

One of the restricted materials is lead, which manufacturers have widely used for more than 50 years as a prime component of solder and connection plating. Unfortunately, lead-free solder alternatives, which use high concentrations of tin, have some drawbacks that make them more difficult and costly to use than traditional solder formulas. These drawbacks include higher melting temperatures, greater rigidity, and lower surface tension when liquid, which affects the solder's ability to pull surface-mount components into alignment. One major concern regarding tin-based plating is its tendency to generate microscopic extrusions, or whiskers, from surfaces after manufacturing. These whiskers can grow long enough to form short circuits in fine-pitch packaging and can break off to contaminate pc boards.

With all these drawbacks, it is no wonder that the electronics industry did not willingly switch to lead-free solder; it took regulatory pressure to force the changeover. The problem is that the regulatory pressure is not the same across all industries. The ROHS directive's prime focus is consumer electronics. As a result, the directive temporarily or permanently exempts several product classes, including networking equipment and industrial products for installation in manufacturing facilities (see **sidebar** "Out from under ROHS").

This uneven regulatory pressure combines with the drawbacks of lead-free solders to create a market full of a mixture of leaded and lead-free components. The ROHS restrictions on materials such as cadmium, mercury, hexavalent chromium, and flame retardants produce a similarly mixed market for wires and cables, chassis platings, and packaging materials.

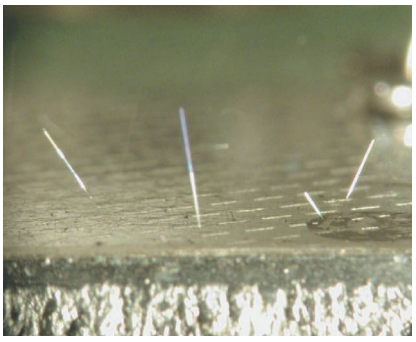
## AT A GLANCE

- The ROHS (reduction-of-hazardous-substances) initiative goes into effect July 1, 2006, and restricts the use of six hazardous materials in electronic equipment, including lead in solder.
- Inconsistent parts availability and ambiguous parts-identification schemes create significant challenges for developers trying to qualify their designs as ROHS-compliant.
- Designers need to look beyond the parts to assess the impact of process changes on their design rules.
- Accounting for environmental regulations is becoming a permanent part of the design task.

The existence of a mixed market generates two of the greatest challenges facing design engineers seeking to develop ROHS-compliant products: finding parts and ensuring their compliance. Design teams are discovering that the time and effort necessary for qualifying parts for new, ROHS-compliant designs are significantly greater than they expected. That unexpected effort, along with confusion regarding exemptions, leaves some design teams scrambling to implement the ROHS directive.

Machine-vision developer Cognex represents a typical case. "When we first looked at ROHS we thought we were exempt," says Cognex hardware engineer Reza Vahedi, "but we were not convinced, so we started converting to compliant designs about 18 months ago. Later, we started getting a lot of inquiries from our customers saying that their systems needed to be compliant because their end users needed to be compliant." Vahedi reports that, when Cognex began trying to qualify components, it found no consistency among vendors in part-numbering or order-identification schemes for indicating that a component was ROHS compliant. Documentation from vendors for validating component compliance was also inconsistent.

Many design teams report similar difficulties. Michael Allen, director of engineering at Bear Power Supplies, says, "Sourcing has been a real challenge. Some companies list a ROHS part number, but it turns out they haven't started making it yet, so there are none in captivity." Allen notes that many fundamental components for use in both exempt and nonexempt applications are only now becoming available in ROHS-compliant versions and that manufacturers are making other noncompliant components. "You may have parts you have used for 16 years, such as a favorite fuse, that are just coming out in a ROHS version. But production lines have to be compliant now to meet the July 1 deadline, so design engineers are scrambling to identify and design in alternatives."



Plating materials containing high concentrations of tin can form whiskers that can cause short circuits and compromise system reliability, so many manufacturers will keep using lead for components in designs not subject to the ROHS directive (courtesy NASA Goddard Space Flight Center).

The result is a significant level of effort on the part of design teams to requalify all of their bills of material or to find alternatives when ROHS versions are unavailable. "It's a laborious process," says Allen. In some cases, he notes, a ROHS version may be available but not in a particular package style, forcing redesign of pc boards.

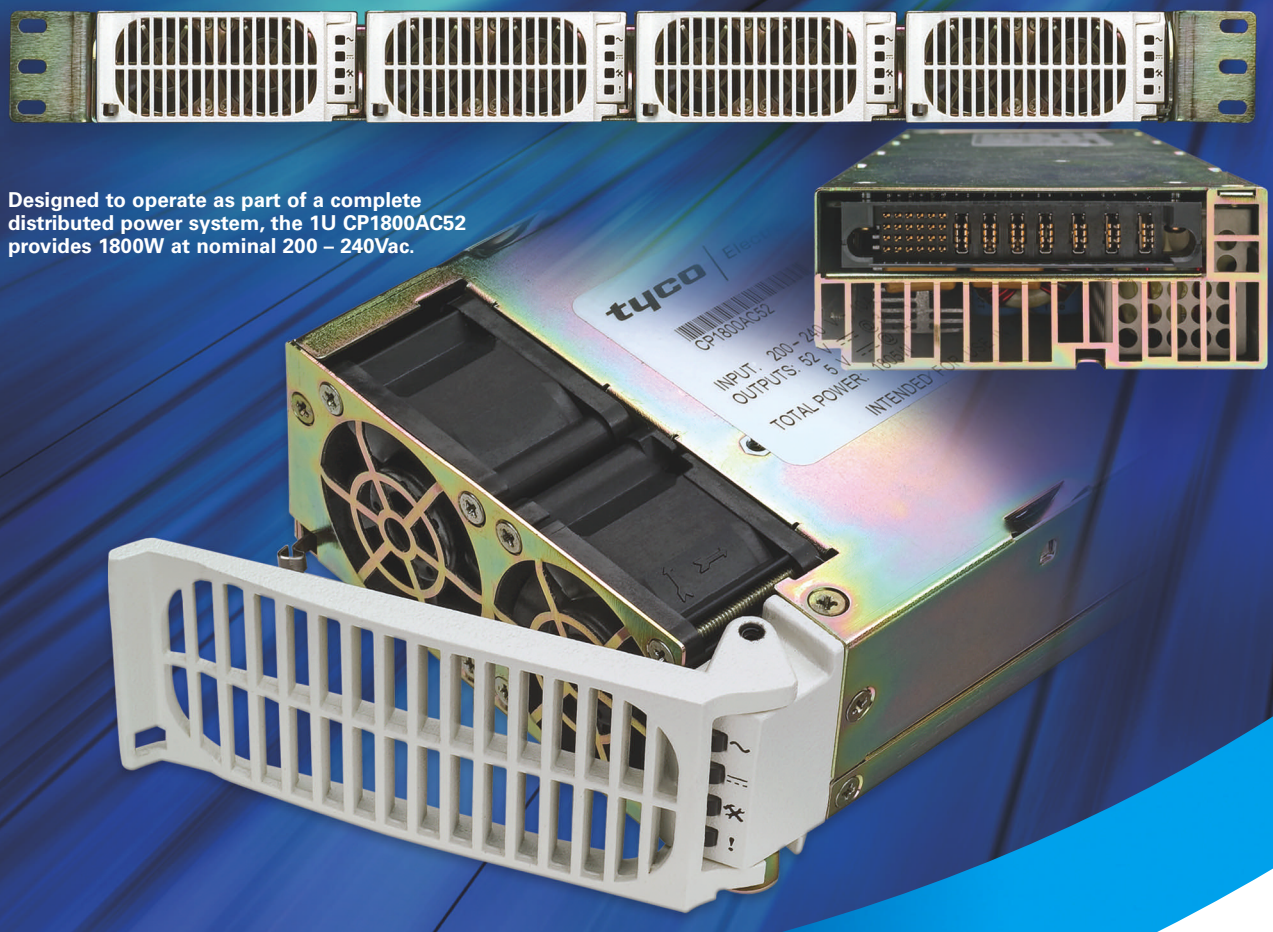
Allen also points out that the parts on distributors' shelves and elsewhere in the supply pipeline might be a mix of compliant and noncompliant versions and

## ROHS IN BRIEF

**The ROHS (reduction-of-hazardous-substances) Directive 2002/95/EC of the European Parliament imposes a restriction on the use of hazardous substances for electrical and electronic equipment within the European Union. The directive bans the use of lead, mercury, cadmium, hexavalent chromium, PBBs (polybrominated biphenyls), and PBDEs (polybrominated diphenyl ethers). Amendment 2005/618/EC clarifies the restrictions to indicate that the maximum concentration by weight in a homogeneous material for these substances is 0.01% for cadmium and 0.1% for all others.**

**This directive impacts the design and manufacture of electronic equipment in both obvious and subtle ways because of the widespread use of these materials. For example, lead has long been a significant component of solder and component plating. Mercury is a component of products as diverse as reed relays and fluorescent lighting. Cadmium finds use in batteries and photo sensors, as well as in wires and cables. Hexavalent chromium sees use as a plating material for electronic chassis, and manufacturers commonly use PBBs and PBDEs to make flame-retardant cloth and other materials.**

**Manufacturers selling products in the European Union must comply with the directive as of July 1, 2006. Member countries are free to impose their own penalties for failure to comply.**

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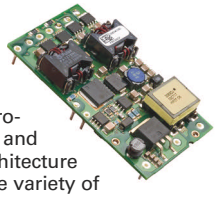

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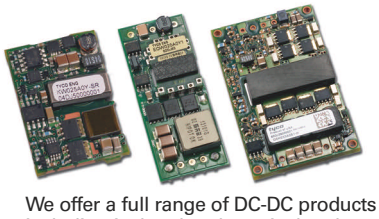

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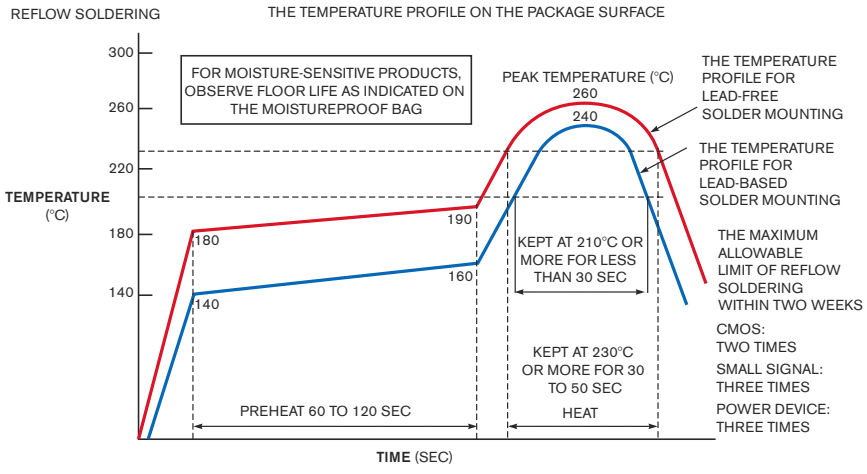


Figure 1 The surface temperature for packages soldered with lead-free materials can be as much as 40°C greater than those packages using leaded solder. This temperature difference can impact board layout and materials handling (courtesy Toshiba America Electronic Components).

that telling them apart can be challenging. "Some companies make ROHS parts, but they do not have new part numbers for them. Manufacturers may be making these ROHS parts at one plant or only after a certain date, so you have to interpret sometimes-cryptic markings to ensure compliance."

The marking issue is equally frustrating for vendors. "Our initial strategy was to not change the part numbers," says Kirk Olund, quality manager at Fairchild Semiconductor. "Making the parts ROHS-compliant had no impact on their electrical or functional performance, so we viewed it as simply being a change to the finish on the lead frame and handled it with a materials-specification-change notice. Because of pushback from our customers, however, we have now created new part numbers."

## PROBLEM TEMPERATURES

Although the electrical performance of lead-free components does not differ from the performance of those with lead, designers still have other differences to consider once they find a ROHS-compliant alternative to use in their designs, Olund notes. Designers must also account for manufacturing-process changes. One of the most significant, Olund says, is the higher temperatures necessary to melt lead-free solders.

Typical soldering profiles for lead-free solder are 20 to 40°C greater than the profiles for lead-based solder. This additional heat during manufacturing can damage

## OUT FROM UNDER ROHS

**The ROHS (reduction-of-hazardous-substances) directive allows for numerous exceptions and specifies several categories of equipment that need not comply. These exceptions include mercury in several types of fluorescent lamps; lead in CRT and fluorescent-lamp-tube glass; lead in solder for servers, storage, and storage-array systems (until 2010); and lead in solder for network-infrastructure equipment. In addition, the legislation does not apply to large-scale stationary industrial tools; spare parts for equipment in service; and electronic equipment that is a component of equipment in a different category, such as a radio in a car. Batteries fall under their own regulations (see sidebar "Green batteries"). An exemption for military equipment is under debate.**

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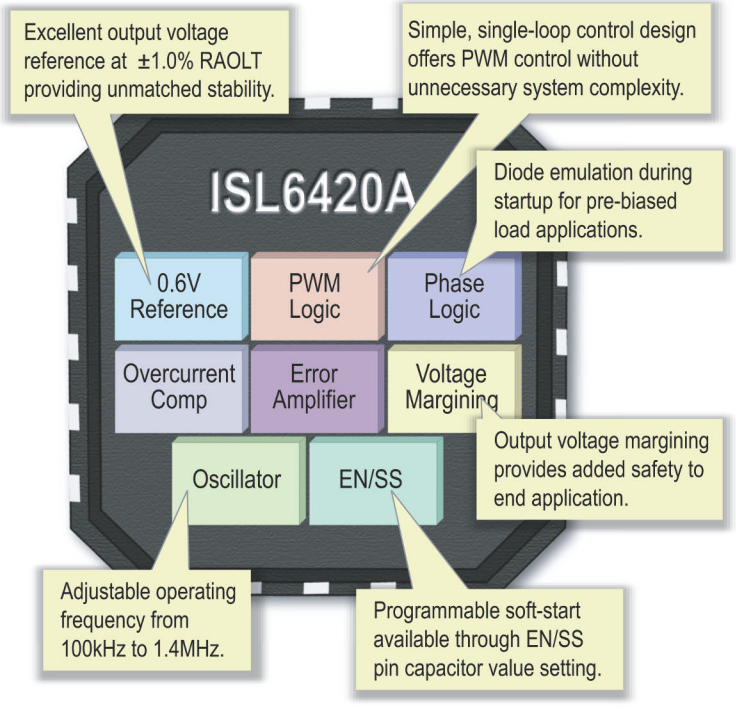


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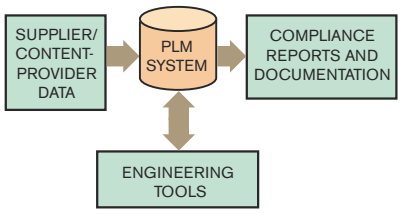
components that are too close to each other. Further, the MLS (moisture-level sensitivity) of packages may be greater at the higher temperatures, requiring special handling of components while in inventory and during manufacturing to prevent moisture absorption that can result in subsequent fracturing during the soldering stage. Design engineers are typically responsible for specifying the manufacturing conditions, so they need to investigate such details when qualifying parts.

More subtle design changes also exist. Lead-free solders are more rigid than leaded solders, so designers must re-evaluate a design's resistance to vibration and shock when making a ROHS-compliant design. The wicking of liquid solder, which board fabricators use to ensure self-alignment of surface-mount components, has less effect on lead-free alternatives. As a result, the placement of components must include increased error tolerance to avoid mechanical interference and short circuits. Designers must even re-examine pc-board materials. Lead-free manufacturing's higher soldering temperatures can delaminate boards designed to use lead-based soldering.

At first glance, much of the design effort in ensuring ROHS compliance seems to be short-term. Once designers make the effort to alter their design rules and approved component lists, it appears, these new guidelines can become as second nature to them as the original ones and not permanently alter the design effort. The problem with such appearances, however, is that they do not reflect the increasing reach of environmental regulations.

The ROHS directive is only the beginning. Nations such as China and Japan are drafting their own environmental initiatives using ROHS as a template. These initiatives may have different—even




Product-life-cycle-management tools can help designers keep pace with parts-compliance issues by warehousing relevant documents and linking supplier databases to engineering tools (courtesy Omnify Software).

## GREEN BATTERIES

**The materials restrictions of the ROHS (reduction-of-hazardous-substances) directive do not apply to batteries and accumulators. The European Union battery directive 91/157/EEC covers these devices. This directive provides for the collection and recycling of batteries containing lead, mercury, or cadmium and requires that batteries built into equipment be removable for recycling.**

**However, battery packs are not totally immune to the ROHS restrictions. According to Todd Sweetland, engineering manager at MicroPower, the pc boards and charging circuits in battery packs must still meet ROHS guidelines. The battery directive covers only the batteries themselves.**

**The directive is also changing. The EU technical committees are updating the directive and will impose more stringent restrictions. The emerging directive will effectively ban batteries containing mercury and cadmium in most products, although medical, military, and space equipment will be exempt. The cadmium ban also allows an exemption for emergency and alarm systems as well as a four-year exemption for power tools.**

**Some topics under negotiation include a requirement that users can readily remove batteries from equipment and a provision that producers finance public-awareness campaigns to support recycling efforts. Recycling guidelines are also unsettled; proposals range from a goal of successfully recycling 25 to 45% by weight of batteries sold.**

**The EU technical committees expect to finalize the new directive by June 2006 and for member states to implement it within two years of finalization.**

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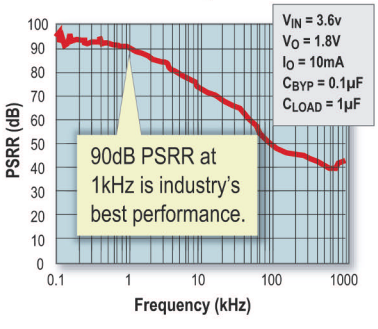
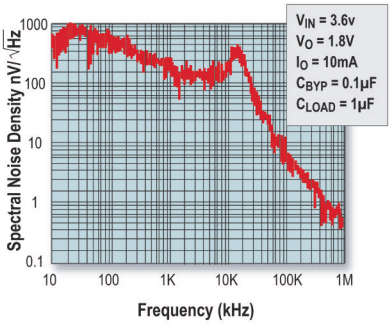
**ISL9000 PSRR (POWER SUPPLY REJECTION RATIO) vs FREQUENCY**




**ISL9000 SPECTRAL NOISE DENSITY vs FREQUENCY**

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**Low Dropout Regulator Selection Table**

| | PSRR at 1kHz | Output Noise Vrms @ 100µA (1.5V) | $I_{OUT}1$ (max) mA | $I_{OUT}2$ (max) mA | $I_Q$ (typ) µA | Voltage Accuracy |
|---|---|---|---|---|---|---|
| **ISL9000** | 90dB | 30µ | 300 | 300 | 42 | 1.8% |
| **ISL9007** | 75dB | 30µ | 400 | - | 50 | 1.8% |
| **ISL9011** | 70dB | 30µ | 150 | 300 | 45 | 1.8% |
| **ISL9012** | 70dB | 30µ | 150 | 300 | 45 | 1.8% |
| **ISL9014** | 70dB | 30µ | 300 | 300 | 45 | 1.8% |

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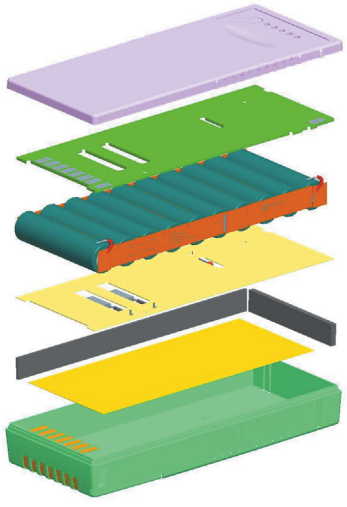
harsher—restrictions. In addition, standards bodies may eventually phase out the exemptions that ROHS currently allows. Some exemptions now have expiration deadlines. As a result, the issue of parts compliance will arise repeatedly, and designers will need to continually re-evaluate design rules and approved vendor lists to keep pace.

According to Blair Davies, director of global-design services at contract manufacturer Celestica, design engineers will need to work to keep their approved parts lists up to date. "Designers have to know a lot more than they did before," says Davies. "They have to be more involved in the selection of components. They can no longer just design-in parts and leave the rest to manufacturing. If they do, they risk designing in obsolescence as regulations and parts availability change."

One way of handling this ongoing need is to use a PLM (product-life-cycle-management) tool for tracking parts compliance as regulations change. Tools such as PLM from Omnify Software can provide a repository for documentation and data for requalifying parts when necessary. "Designers have to be cognizant of these initiatives," says Chuck Cimalore, Omnify's chief technical officer. "They also need product data and the tools to handle that data to protect themselves by keeping their qualified parts lists current."

Unfortunately, the information designers need to determine compliance as rules change may not be readily available. Cimalore notes that, although his company's tool can store compliance reports and other documentation, as well as automatically compare component data with design guidelines as regulations evolve, vendors are inconsistent in the type and format of the information they provide. Some simply provide certificates of compliance rather than full materials specifications, and others provide only partial information. "Design teams need to get their vendors to provide them the information they need," says Cimalore.

Over time, the practices and standards within the electronics industry for handling environmental concerns may finally resolve themselves. Most design teams, however, expect that this resolution will take at least several years. Meanwhile, designers will have to adapt by becoming more involved in parts qualification and in assessing the impact of process changes. Because, whether they like it or not, green design is becoming the way of the world in electronics. EDN



The batteries in battery packs are exempt from the ROHS directive, but the charging circuits and other elements of the pack may not be (courtesy MicroPower).

## AUTHOR'S BIOGRAPHY

*Contributing Technical Editor Richard Quinnell has been covering technology for more than 15 years. He has been a practicing engineer in embedded systems and has degrees in engineering and applied physics.*

## FOR MORE INFORMATION

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## MORE ROHS COVERAGE

**The March issue of *EDN*'s sister publication, *Electronic Business*, includes a ROHS feature that addresses the cost to the OEM, implications in the supply chain, exemptions from compliance, and how some companies hope to offset the cost of ROHS through premium customer services. Read the article at www.eb-mag.com/ROHScosts.**

TEXAS INSTRUMENTS

DATA CONVERTERS

Analog Applications Journal

BRIEF

# Operating multiple oversampling data converters

*By Joe Purvis • Data Acquisition Products*

## 1.1 Introduction

This article discusses some important considerations that should be taken into account during the design of a simultaneous sampling system using oversampling data converters. The ADS1252 ADC is used as an example.

To successfully use oversampling data converters in a simultaneous application, the modulator clock (MCLK) for each ADC must be shared. This assures that each converter is truly sampling the inputs concurrently. It has the added benefit of simplifying the digital interface since only one interrupt pin is required, regardless of the number of ADCs in the system.

However, a significant limitation is that there is a fixed amount of time—348 MCLK periods—available to read the converted data. After this fixed time, the data output register is being updated with a new data word regardless of whether the data has been read or not.

The converted data is read from the device using a shift-clock (SCLK) generated via the host system. There is no direct relationship between MCLK and SCLK, but the user should be aware that if the data is not shifted out of the ADC quickly enough $T_{DOUT}$ time will expire and the data read back will be a meaningless mixture of old and new data. This should be carefully considered, particularly where multiple ADCs are concerned.

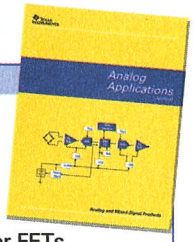
## 1.2 Oversampling catch

Oversampling data converters generally have better ac and dc specifications than Successive Approximation Register (SAR) based converters. But SARs do have one fundamental advantage, namely on command from the host, SAR converters are able to complete and deliver one measurement.

In comparison, oversampling architectures by their nature rely upon averaging repeated coarse measurements before arriving at a final value. The architecture details are beyond the scope of this paper, but it is essential to appreciate this point in order to successfully use oversampling converters.

## 2 Data transfer principles

The preliminary details in support of this application note are contained in the application note, Interfacing the ADS1251/52 to the MSP430, SLAA242. It is recommended that the reader should first read this application note to gain an understanding of the device's operation.



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## 2.1 Modulator clock (MCLK)

The modulator clock applied to the ADS1252 ADC is the principle driver used to set the characteristics of the ADC. The two properties that MCLK provide are the frequency response of the ADC and also the frequency at which the ADC indicates new data is available.

The modulator clock period ($t_{MCLK}$) is defined as

$$\tau_{MCLK} = \frac{1}{MCLK} \quad \text{Equation (1)}$$

## 2.2 Digital Interface

To briefly recap the operation of the digital interface from the datasheet, there is only one data output pin. The function of this pin is multiplexed between DOUT and DRDY. A complete conversion consumes 384 MCLK cycles. The cycle is divided into two phases (Figure 1).

The first phase of the cycle is known as DRDY mode. Following the $T_{DOUT}$ time, the rising edge of the DOUT/DRDY signal indicates that new data will be available in 36 MCLKs. During this time, the data output register is updated. This signal is connected to an interrupt pin on the host system.

The second phase of 348 MCLKs is known as DOUT mode. During this time, the user can safely read the converted data at a clock rate determined by the shift clock (SCLK).

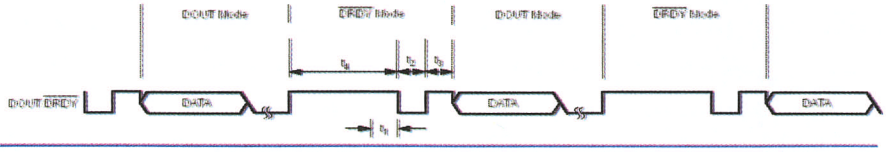


Figure 1

## 2.3 A tale of two clocks

Regardless of the number of ADCs, the same principle of DOUT/DRDY time must still be adhered to for the ADS1252. In general, for N data converters, the time allocated for DOUT mode can be expressed as:

$$T_{DOUT(N)} = \frac{348 * \tau_{MCLK}}{N} \text{ (s)} \quad \text{Equation (2)}$$

The maximum modulator clock (MCLK) for the ADS1252 is specified as 16MHz. Therefore $t_{MCLK}$ is 62.5ns, and $T_{DOUT}$ can be re-written as

$$T_{DOUT(N)} = \frac{21.75 \times 10^{-6}}{N} \text{ (s)} \quad \text{Equation (3)}$$

Figure 2 shows both SCLK signals and both DOUT/DRDY signals required to read data from two ADCs.

As the number of ADCs sharing the same modulator clock increases, the DRDY period stays the same, but the data from each ADC must be accessed faster.

To receive the complete 24 bits from each ADC requires 3 x 8-bit accesses, 24 SCLKs in total. Therefore to be able to access the data from N ADCs requires a time of N x 24 SCLKs. It is the user's responsibility to ensure that all accesses are complete prior to the next DRDY time.

An alternative approach would be to verify the maximum speed offered by the host system for SCLK, 2MHz for example, and then determine how long it would take to transfer 24 bits of data at that clock speed; this would determine the maximum modulator clock frequency that could be used. In a multiple ADC system, if the modulator clock is faster than the calculated maximum, there will not be enough time for the host to read the data before the ADC switches from DOUT mode to DRDY mode.

For example, if $t_{SCLK}$ = 500ns then 24 x $t_{SCLK}$ = 12µs for 24 bits of data. This indicates that it will take at least 12µs to clock the data out of any ADC (this sets $T_{DOUT}$), consequently if there are 5 ADCs sampling data synchronously, it will take at least 5 x 12µs (60µs) until the system can read the first ADC again.

Therefore, according to equation 2, the maximum modulator clock will be 5.8MHz.

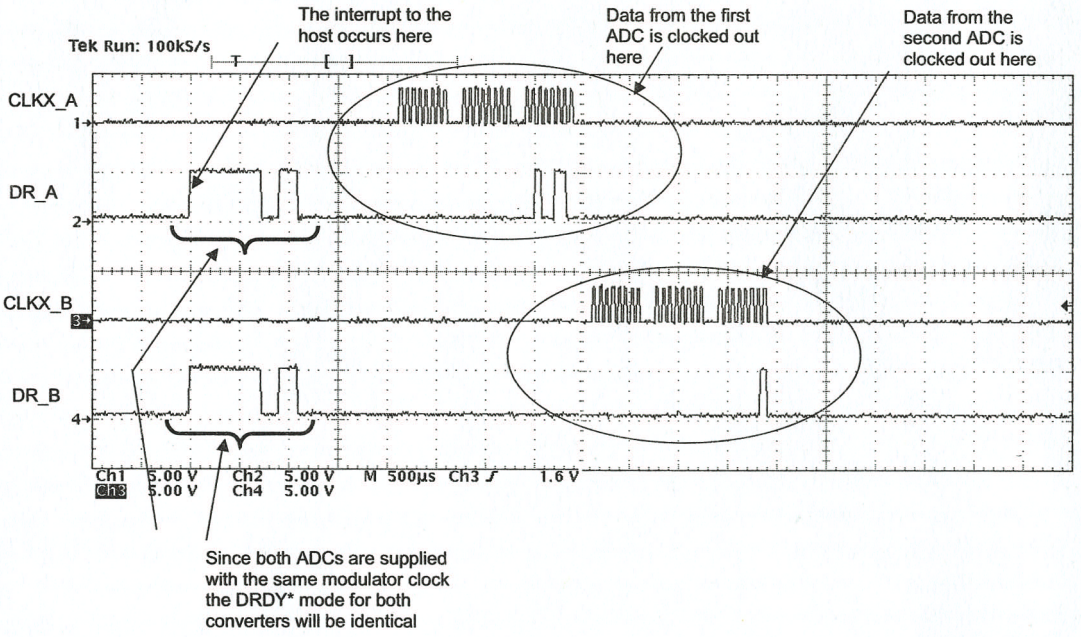


Figure 2– A composite from two adjacent screen captures showing CLKX_A, DR_A, CLKX_B and DR_B

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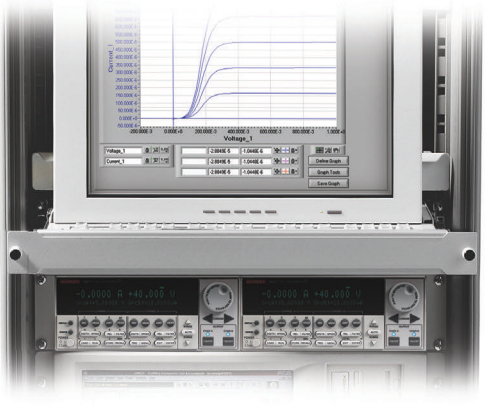

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BY MARGERY CONNER • TECHNICAL EDITOR

# Wireless-sensor networks

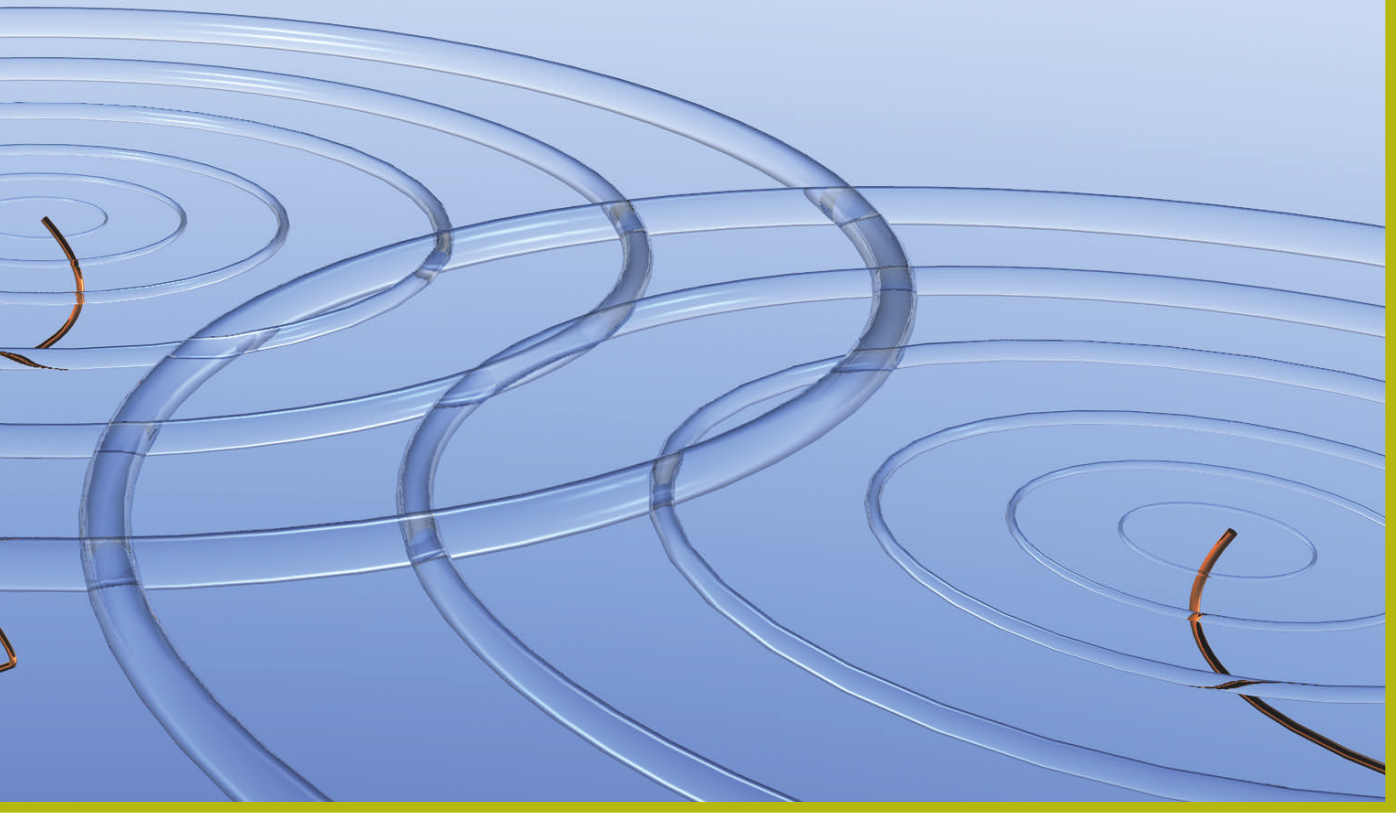
## find a fit in the unlicensed band

WELCOME TO THE NEW WORLD OF WIRELESS CONNECTIVITY, THANKS TO RECENTLY INTRODUCED STANDARDS, PROTOCOLS, AND ENABLING HARDWARE FOR THE UNLICENSED RF BANDS.

Low-power, short-range, low-data-rate wireless networks use the unlicensed RF band. In addition to their overriding need to operate on severely constrained energy sources, such as using one battery for their entire lifetimes or employing energy they scavenge from the environment, these networks must contend with interference from sources such as Bluetooth headsets and microwave ovens. These networks use network protocols that largely determine the networks' efficiency, robustness, and security. As such, network designers need to first determine which sub-band is best for their application: 900 MHz or 2.4 GHz. In addition to selecting the frequency band, they also need to decide on a hardware-transceiver scheme: a roll-your-own or an SOC (system-on-chip) approach. They must also decide which network protocol to use.

Both the 900-MHz and 2.4-GHz bands have advantages. Both reside in the ISM (industrial/scientific/medical) band, an unlicensed frequency band of 902 to 928 MHz, 2.4 to 2.483 GHz, and 5.725 to 5.875 GHz. Almost all of the transceiver and SOC products targeting wireless-sensor-network applications use the 900- to 928-MHz and 2.4- to 2.483-GHz bands. The 900-MHz band touts long broadcast range because of its relatively longer wavelength and its correspondingly longer battery life. However, lower frequency means the use of a larger antenna than a 2.4-GHz system requires. And, if you plan to sell your system into a global market, you will quickly encounter a lack of standardization in the 900-MHz range. For example, in Europe, you cannot use the 900- to 928-MHz band because it is part of the GSM (Global System for Mobile communications) network for cell-phone communication and, thus, is unavailable.

Wireless-sensor-network-system pioneers, such as Aerocomm, Dust Networks, and Crossbow Technologies, take different approaches to these constraints. For example, Aerocomm sells wireless-network systems into the global market, offering different radios and frequencies for different regions. Randy Macke, international marketing manager at the company, explains, "We typically use 2.4 GHz for higher-data-rate applications at short range. The flip side is when you go to a 900-MHz product family, there is better range performance but typically a slower data rate. These are the basic trade-offs." He says that the company aims at making



## AT A GLANCE

- Wireless-sensor networks have tight power-consumption and network-resiliency specs.
- You must choose between 900 MHz and 2.4 GHz in the unlicensed ISM (industrial/scientific/medical) band.
- The frequency band you choose depends on which countries you want to sell to, your power constraints, how far you want to broadcast, and your data-transmission rates.

its products global by using one proprietary protocol and interface on every radio it sells; hence, a customer can base a product on Aerocomm's 900-MHz product and then sell into another country that doesn't accept 900 MHz just by swapping in a pin-compatible radio.

David Boylan, marketing manager for Analog Devices, also recommends this approach. Boylan sees companies opting for the 900-MHz or the 2.4-GHz frequencies because of the technical attributes of the two bands and whether these companies need to adapt to a proprietary or a standard network. According to Boylan, vendors often choose the 2.4-GHz band because either the vendor or its customers like the security of standards. But this preference is not universal. Other companies prefer to create their own proprietary networks, he says. Reasons for this preference are the value-added and security aspects of proprietary networks. "If they have their own proprietary network, they can implement security features that wouldn't be available in a published standard," Boylan says. These vendors typically prefer to use frequencies of less than 1 GHz, such as 900 MHz (**Table 1**).

He cites as an example a popular 900-MHz application of an automatic meter reader. "You usually have a central node, which might be the utility employee with his handheld unit pinging several units. The 900-MHz band is popular because range and battery power are key requirements," says Boylan. For networks relying on tiny sensor nodes, the 900-MHz antenna of approximately 8 cm is probably too large. In this case, even if your market is 900-MHz-friendly North America, you may need to consider 2.4 GHz because of its smaller antenna (see **sidebar** "Antenna technology feels the squeeze"). Airtime also affects power consumption. Wireless-


This kit from Microchip is a low-cost entry into developing low-power, low-data-rate wireless networks. Other than the included Zigbee-protocol stack, the software is not Zigbee-centric. The kit includes two PICdem Z boards, each with an RF daughtercard, as well as a Zigbee stack.

**TABLE 1 TRANSCEIVERS AND SOCs FOR LOW-DATA-RATE NETWORKS**

| Vendor | Part no. | Frequency bands | Modulation format | Transmitting current at 0 dBm (mA) | Receiving current (mA) | Output-power range (dBm) | Supply range (V) |
|---|---|---|---|---|---|---|---|
| Analog Devices | ADF7020 | 431 to 478 MHz, 862 to 956 MHz | GFSK/FSK/ASK/OOK | 19.1 | 19 | 13 | 2.3. to 3.6 |
| Analog Devices | ADF7020-1 | 135 to 650 MHz | GFSK/FSK/ASK/OOK | 18.6 | 18.5 | 13 | 2.3 to 3.6 |
| Analog Devices | ADF7021-1 | 135 to 650 MHz | GFSK/FSK/ASK/OOK | 18.6 | 18.5 | 13 | 2.3 to 3.6 |
| Atmel | ATA5429 | 915 MHz | FSK/OOK | 9.6 | 10 | 10 | 2.4 to 3.6 |
| Ember | EM250 | 2.4 GHz | O-QPSK | 35 | 35 | As high as 4 | 2.3 to 3.6 |
| Freescale | MC13202 | 2.4 GHz | O-QPSK | 30 | 37 | −27 to +4 | 2 to 3.4 |
| Freescale | MC13211 | 2.4 GHz | O-QPSK | 30 | 37 | −27 to +4 | 2 to 3.4 |
| Freescale | MC13212 | 2.4 GHz | O-QPSK | 30 | 37 | −27 to +4 | 2 to 3.4 |
| Freescale | MC13213 | 2.4 GHz | O-QPSK | 30 | 37 | −27 to +4 | 2 to 3.4 |
| Texas Instruments | CC1100 | 315, 433, 868, 915 MHz | FSK, OOK, MSK | 16.6 | 15.1 | −30 to +10 | 1.8 to 3.6 |
| Texas Instruments | CC1110 | 315, 433, 868, 915 MHz | FSK, OOK, MSK | 31 | 22 | −30 to +10 | 2 to 3.4 |
| Texas Instruments | CC2420 | 2.4 GHz | DSSS (IEEE 802.15.4) | 17.4 | 19.7 | −20 to 0 | 2.1 to 3.6 |
| Texas Instruments | CC2430 | 2.4 GHz | DSSS (IEEE 802.15.4) | 24.7 | 27 | −20 to 0 | 2 to 3.6 |
| Texas Instruments | CC1020 | 433, 868, 915 MHz | FSK, OOK, GFSK | 20.5 | 19.9 | −20 to +10 | 2.3 to 3.6 |


Freescale's MC1320X Zigbee SIP (system in package) combines an HCS08 microcontroller and a 2.4-GHz transceiver in a single 64-pin QFN package. The package also includes features, such as a 10-bit ADC and embedded flash memory.

## ANTENNA TECHNOLOGY FEELS THE SQUEEZE

**You must budget the cost and size of antennas into your wireless design. Your options include whip, pc-board, and chip antennas. Whip antennas are familiar additions to mobile wireless devices, such as cell phones, wireless handsets, and walkie-talkies. The formula L=7500/frequency (MHz) provides a good approximation for a quarter-wavelength whip antenna for low-power systems, yielding 8.33 cm for a 900-MHz system (Reference A).**

**An antenna can also be a trace on a pc board, which has the benefit of adding virtually no cost. However, you must exercise care in using a pc-board antenna, according to George Rueter, senior applications engineer for Atmel. He says that designers often overlook the issue of antenna selection. Selecting the right antenna provides an advantage in both transmitting and receiving. "If you choose the right antenna, you can pick up a couple of decibels of gain," he says.**

**Chip antennas can provide excellent reception and transmission capabilities but at an additional cost of approximately $1. Chip-antenna vendors include Fractus, gigaAnt, and Murata.**

**REFERENCE**

**A Smith, Kent, "Antennas for low power-applications," www.web-ee.com/primers/files/antenna.pdf.**

sensor networks conserve power by spending 99.99% of their time asleep, and they wake up only to contact their network and briefly transmit their information, thus achieving their goal of consuming an average of less than 1 μA of current (**Reference 1**). Therefore, the faster they can transmit their data, the more quickly they can go off the air. This point favors the use of the 2.4-GHz spectrum.

Dust Networks develops both the hardware and the software for companies needing wireless-sensor networks. Dust makes 802.15.4-compliant products in the 2.4-GHz band and in the proprietary-network, 900-MHz band. Many customers use the 900-MHz network devices for building automation. For this appli-

| Sensitivity (dBm) | Approximate line-of-sight range (m) | Maximum data rate (kbps) | Included functions | Price (1000) | Package |
|---|---|---|---|---|---|
| −112 | NA | 200 | NA | $2.29 | 7×7-mm, 48-lead LFCSP |
| −114 | NA | 200 | NA | $2.20 | 7×7-mm, 48-lead LFCSP |
| −117 | NA | 25 | NA | NA | 7×7-mm, 48-lead LFCSP |
| −107 | 800 | 40 | Demodulation and transceiver/receiver byte buffer | $3 | 7×7-mm QFN-48 |
| −97 | NA | 250 | 16-bit XAP core with 128-kbyte flash memory, 5-kbyte RAM, two timers, sigma-delta ADC, integrated encryption core | $5 | 7×7-mm QLP-48 |
| −94 at 1% packet-error rate | 400 | 250 | External | $2.75 | 5×5-mm QFN-32 ROHS |
| −94 at 1% packet-error rate | NA | 250 | 8-bit Freescale microcontroller with 16-kbyte flash and 1-kbyte RAM | $3.61 | 9×9-mm LGA-64 ROHS |
| −94 at 1% packet-error rate | NA | 250 | 8-bit Freescale microcontroller with 32-kbyte flash and 2-kbyte RAM | $3.94 | 9×9-mm LGA-64 ROHS |
| −94 at 1% packet-error rate | NA | 250 | 8-bit Freescale microcontroller with 60-kbyte flash and 4-kbyte RAM | $4.32 | 9×9-mm LGA-64 RoHS |
| −110 | 500 | 500 | 2×64-byte FIFO, packet handling, addressing, wake-on radio | $1.83 | 4×4-mm QLP-20 |
| −109 | 500 | 500 | SOC with 8051 microcontroller, 32-kbyte flash, 4-kbyte RAM, Advanced Encryption Standard | $4.64 | 6×6-mm QLP-36 |
| −94 | 100 | 250 | 2×128-byte FIFO, packet handling, addressing | $3.60 | 7×7-mm QLP-48 |
| −94 | 100 | 250 | SOC with 8051 microcontroller, 128-kbyte flash, 8-kbyte RAM, Advanced Encryption Standard | $5.80 | 7×7-mm QLP-48 |
| −118 | 1200 | 153.6 | Bit synchronizer, automatic frequency compensation | $4.43 | 7×7-mm QFN-32 |

cation, says Rob Conant, Dust's chief executive officer, the 900-MHz band presents a technical advantage because of its longer range and better penetration in buildings, which allows lower power consumption (**Reference 2**). As for the marketing side of the equation, Conant believes that the 2.4-GHz band has an edge. "The global ISM band is the only way to go for companies that want to bring out global products," he says. "Although 2.4-GHz products suffer a penalty in power consumption to get the same range [as 900 MHz], 2.4 GHz is a standard, and customers know it's going to be around for years."

Karl Torvmark, strategic product-marketing manager for Chipcon, agrees. Chipcon's 2.4-GHz Zigbee devices reach 100m or more in good conditions, he says. For a longer communications range, you can increase the output power beyond 1 mW, but doing so directly affects the power consumption. If you go below 1 GHz with the same output power, you reach several hundred meters, but then an antenna issue arises. "In the hundreds of megahertz, you like to have a whip antenna, usually mounted externally ... if that's compatible with your overall product design," he says. Although you can use pc-board antennas operating at less than 1 GHz, they can be impractically big," he states.

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Torvmark sees customers leaning toward custom protocols selecting 900 MHz, just as ADI's Boylan does. Chipcon's customers want to customize their networks, which provides advantages and trade-offs in power consumption, he says. For example, Chipcon's 900-MHz-band products, the CC1100 and the higher performance CC1020, don't offer the total network stack that the 2.4-GHz Zigbee products have.

Although Dust's Conant is a steadfast proponent of the 802.15.4 standard, he's not jumping on the Zigbee-protocol bandwagon: He sees severe limitations to Zigbee for ultralow-power wireless-sensor networks. He gives an example of one instance in which the Zigbee standard uses a less reliable approach than he

## A BRIEF GUIDE TO 802.15.4 AND NETWORK PROTOCOLS

**IEEE 802.15.4 governs the low-level layers of wireless short-range PANs (personal-area networks) in the unlicensed RF band for low-power, low-bandwidth applications, such as wireless-sensor networks, interactive toys, and home automation. "Low-level" refers to the lowest two levels of the OSI (Open Systems Interconnection) networking-reference model: the MAC (media-access control) and PHY (physical) layers. The specification stipulates such features for the communication scheme as 250-, 40-, or 20-kbps data rates, depending on bandwidth; 16, 10, or one channel; and the handshaking protocol. These specifications allow for an effective communication method between two compliant devices.**

**However, networks of devices need a higher level networking protocol. Almost all RF transceivers in the 2.4-GHz band and many in the 900-MHz band claim to comply with 802.15.4, but a controversy exists concerning the selection of a higher level protocol: proprietary, Zigbee, and open-source TinyOS.**

**Many networking-system companies have developed their own proprietary protocols, both as value-added extensions and to allow for unique features, such as frequency hopping. Dust Networks Chief Executive Officer Rob Conant claims that the company's SmartMesh-XR platform delivers 99.99% reliability due to its frequency-hopping capability. "If you rely on a single frequency, and the convenience store next door turns on a Wi-Fi-access point, your system will fall apart. We use frequency hopping to spread out the signal over the entire band."**

**The Zigbee Alliance, a group of member companies that work to define the network-, security-, and application-software layers for 802.15.4 networks, developed the Zigbee protocol. Although the specification is freely available, only Zigbee Alliance members can use it for commercial purposes.**

**The University of California–Berkeley leads the consortium that developed the TinyOS event-based operating environment for wireless-sensor networks. TinyOS works with Zigbee, because Zigbee defines specifications only down to the network layer. For example, a Zigbee network layer could reside on a TinyOS MAC layer. Some companies, such as wireless-network-system vendor Crossbow Technology, use TinyOS for both an operating environment and a network protocol. TinyOS has the added advantage of being open-source software. Table A summarizes the higher level protocols associated with the IEEE wireless-communication standards for the unlicensed band.**

TABLE A HIGH-LEVEL IEEE PROTOCOLS

| Standard | Application | Industry-sponsored protocols |
|---|---|---|
| 802.11b/g/a | Wireless LAN | Wi-Fi |
| 802.15.1 | Wireless PAN, short-range RF-based connectivity for portable personal devices | Bluetooth |
| 802.15.3 | Wireless greater-than-20-Mbps PAN | WiMedia |
| 802.15.4 | Low power, low data rate | Zigbee |

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claims Dust can achieve using its own 802.15.4-compliant network, SmartMesh. "An 802.15.4 radio has 16 channels. Zigbee uses only one of those channels at a time. It's configurable which channel you use, but, you set it up, and it uses only one of those channels," he says. And that channel may be experiencing interference from local devices, such as a nearby Bluetooth headset or a microwave. Dust's network hops between all 16 channels based on external interference, which the company claims results in as much as 99.99% reliability.

Clearly, a range of opinion exists about the best way to handle network protocols for 802.15.4 networks (see **sidebar** "A brief guide to 802.15.4 and network protocols"). The benefits of being a standard-compliant technology combine with the approach's global reach and its use of the 2.4-GHz band to make Zigbee a likely winner. IC vendors Freescale, Ember, and Chipcon have all introduced Zigbee-compliant SOC or SIP (system-in-package) products.

Freescale was an early proponent of 802.15.4 and Zigbee, releasing its 802.15.4 transceiver on a chip the day after the IEEE ratified the specification. However, Jon Adams, director of radio technology and strategy for Freescale, claims that system designers don't want to know how to design a network and applications protocol; they just need the basic digital-radio function. So, the company introduced a software-based configuration tool that lets them develop applications using the 802.15.4 stack. Once Zigbee came along last year, he says, the company recognized that designers also need a function for using that Zigbee stack, so that they could quickly build a Zigbee process without reading 700 pages of the spec. "All of our efforts have been toward creating a one-stop shop," he says. Ember and Chipcon have embraced the same approach.

Ember started out developing wireless-sensor-network systems, such as its proprietary EmberNet, before Zigbee existed. The company was also an early member of the Zigbee Alliance. Vice President of Engineering Skip Ashton explains the importance of a multicompany synergy in developing such a complex mesh: "With Zigbee, in addition to the network, you need an ecosystem of the things around your network," he says. Although one company can provide a network stack, a lot of companies are working on other tools and services in a standards-based environment. Other advantages of Zigbee include interoperability testing, multiple-vendor testing, and the availability of multiple sources. Ember's EM250 SOC combines a 2.4-GHz RF transceiver with a 16-bit XAP core, which Cambridge Consultants developed and Cambridge Silicon Radio uses in its Bluetooth chips. The EM250 also includes two timers, a sigma-delta ADC, a USART, an $I^2C$ port, and an integrated encryption core for the Zigbee security algorithms. The company also offers the EM260, which lacks the processor core, allowing designers to choose their own processor and peripheral controller. Ashton agrees with Zigbee's critics that its developers have yet to address all its deficiencies, but he's confident that they will over time. "There are always migration and backward-compatibility issues," he says. As the Zigbee standard evolves, users will be able to perform upgrades in the field through software updates. EDN

## MORE TO COME

**Now that Margery has taken a high-level look at a variety of low-speed wireless technologies, stay tuned for our April 13 cover story, in which Contributing Technical Editor Dan Strassberg digs deep into Zigbee technology and deployment.**

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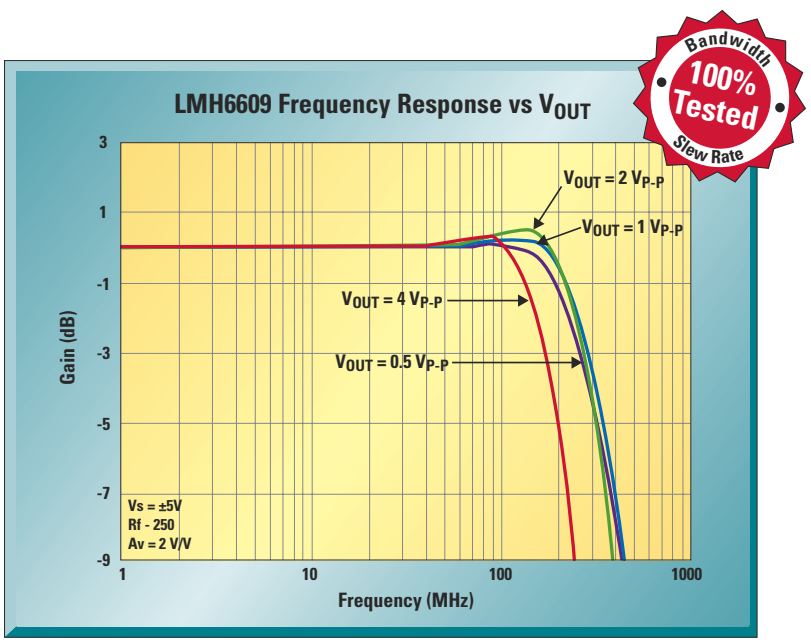


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# System architects get help from emulators

EMULATORS, WHICH DESIGNERS ONCE USED ONLY FOR DEBUGGING AT THE LAST STAGES OF DESIGN IMPLEMENTATION AND FOR REGRESSION TESTING, ARE NOW BECOMING USEFUL TOOLS FOR SYSTEM ARCHITECTS, AS WELL.

Engineers involved in designing leading-edge ICs face a number of difficult challenges. They have to deal with complex physical phenomena on die that require special DFM (design-for-manufacturing) methods and tools, and they have to handle demanding architectural and integration tasks as they plan, develop, and verify the logic design of the IC.

Consumer-electronics and communication devices are the sectors with the greatest vitality in today's electronics market. These products have an average market life of less than one year, and they compete in an aggressive, price-sensitive market; thus, profit margins are low. To be successful in these markets, companies must shorten development time and lower both development and production costs. The result is that the average development time for a leading-edge IC, or SOC (system on chip), is nine months, and its complexity is often greater than the circuits that used to take double the time to develop.

One way companies shorten the design cycle is by reusing functional blocks. This approach has given life to a new segment of the EDA industry: third-party-designed functional blocks. This market segment received the unfortunately chosen abbreviation "IP" (intellectual property), a label that more frequently means Internet Protocol.

## CHALLENGES IN SOC DESIGN

Most SOC devices require engineers to integrate a microprocessor, one or more DSPs, one or more intelligent controllers, some memory, embedded software, and at least one high-speed bus on a single die. In almost all cases, third parties provide some of the functional blocks, most often in the form of hard macros. A hard macro is a black-box circuit. To protect the macro from unauthorized copying, the vendor describes the functions the circuit will perform and the I/O protocol it will use without revealing any information about the internal architecture.

These IP blocks offer a challenge to system integrators because, to protect proprietary information, vendors often provide only a TLM (transaction-level model) of the device. This model is sufficient to verify the interface protocol between the IP and the rest of the system but does not give accurate timing information and may mask errors in the actual data even if the I/O protocol seems to be correct. In addition, engineers face the possibility that the simulation model contains bugs that the vendor has been unable to identify.

When planning a new product, designers begin by listing the required functions. They then partition the product into functional blocks that they will implement in either hardware or software. Engineers implement hardware blocks from scratch, reusing blocks they developed internally, or using third-party IP. The decision to use a third party requires engineers to evaluate the IP, and the process can be time-consuming because they must develop a verification and validation testbench and then evaluate the results. When the only method of evaluating an IP block is to use a simulation model, the results may not represent the actual behavior of the IP because errors can exist in both the model and the testbench.

By increasing the level of abstraction of the models, EDA vendors have given architects a new family of planning tools that allow engineers to simulate the interaction among the various system building blocks before detailed implementation begins. The early proponents of ESL (electronic-system level) predicted that, by using a language that was similar to what software engineers use, architects could more efficiently explore hardware/software trade-offs. Unfortunately, this prediction proved to be only partially true. DFM considerations often require estimating the power consumption of a software block more precisely than is possible using abstract processor models. Software engineers must be able to execute the program as early in the development cycle as possible, so the team can use accurate runtime data to decide on the best architectural configuration.

Once the architecture is final, development of both hardware and software begins. Ideally, the process is concurrent, but, in practice, software development must wait until the hardware that will execute the software is available. Some EDA vendors have offered an approach to the serial nature of this process with

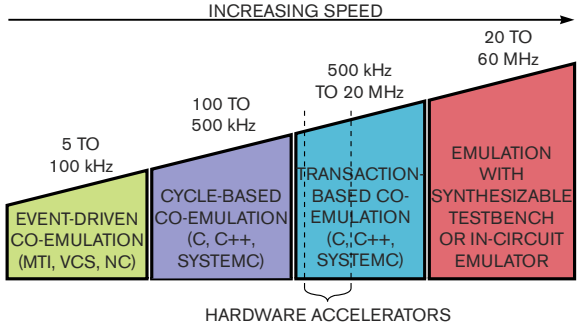


Figure 1 Using more abstract models, hardware accelerators, and emulators increases the speed of digital-logic simulation.

an ISS (instruction-set simulator) that provides a TLM of a processor. Software engineers use the model to validate the algorithmic behavior of their code, but they cannot verify real-time software using an ISS, because the model is not timing-accurate. An ISS model is expensive to build, and engineers can obtain an ISS only for popular embedded processors.

During the development process, engineers must be able to simulate the system using functional blocks at various levels of abstraction. Although they can describe some blocks only at the algorithmic level, the development of others progresses to the RTL (register-transfer level) and readies them for synthesis. Using a logic simulator to validate the design, which contains many RTL blocks, is time-consuming and expensive. If the verification of software implementations requires RTL blocks, the throughput of a logic simulator is so low as to make the approach unrealistic.

## HARDWARE EMULATION IN SYSTEM DESIGN

Although ISS models, TLMs, and pure C or C++ models all provide system designers with the means to evaluate basic system architectures to partition the design, they fail to support analysis in the time domain. These models purposely lack timing models because the major directive in developing these models is to ensure the fastest possible simulation throughput. But most embedded software is time-sensitive, and communications among the various hardware blocks must involve synchronization in time. Waiting for an RTL representation of the design to verify timing is impractical for two reasons. The simulation of RTL circuits is significantly slower than using more abstract models. The resulting delay in verifying software significantly increases development time, causing greater NRE (nonrecurring-engineering) costs and possibly pushing the product beyond its market window.

EDA vendors have addressed the throughput problem by creating hardware accelerators that compile the circuit into hardware primitives. EDA companies such as Cadence (www.cadence.com), Mentor (www.mentor.com), and Tharas Systems (www.tharas.com) market hardware accelerators that provide adequate execution speed but at a significant cost. These hardware boxes can increase the gate-level throughput of a logic simulator by 1000 times, but their cost can run to millions of dollars, which makes them unaffordable to many companies.

**Figure 1** shows how simulation performance increases when you apply various simulation methods. Hardware acceleration improves event-driven simulation so that the throughput is now equal to the lower band of transaction-based co-emulation. Hardware accelerators provide the best productivity improvement when the verification team uses them for regression testing.

**TODAY'S EMULATORS CAN COMMUNICATE WITH A SOFTWARE SIMULATOR AND ALLOW DESIGNERS TO USE ALL THE MODELS THAT THE SOFTWARE SIMULATOR SUPPORTS.**

Another approach is to use a hardware emulator. Emulators allow designers to implement a circuit using FPGA devices instead of an ASIC, thereby running simulations of the circuit at a much higher throughput than a software simulator can provide. When emulators first became available, all of the circuit had to reside in FPGAs, but today's emulators can communicate with a software simulator and allow designers to use all the models that the software simulator supports. The sophistication of emulators has also improved significantly. **Figure 2** shows the architecture of the Zebu-UF, the latest emulator from EVE (www.eve-usa.com). System architects can perform a number of valuable tasks using an emulator with its capabilities.

One factor holding back the growth of the IP market is the inability of potential users to evaluate an IP core without entering into a contract with the vendor. Using a TLM of the core is inefficient. The IP vendor must develop and maintain the model. A vendor cannot distribute the model it used internally to develop the IP because the purpose of the evaluation model differs from the internally developed models. Engineers unfamiliar with the architecture of the commercially available TLM must be able to easily use it. It must be abstract enough to ensure fast simulation, and it must provide an accurate representation

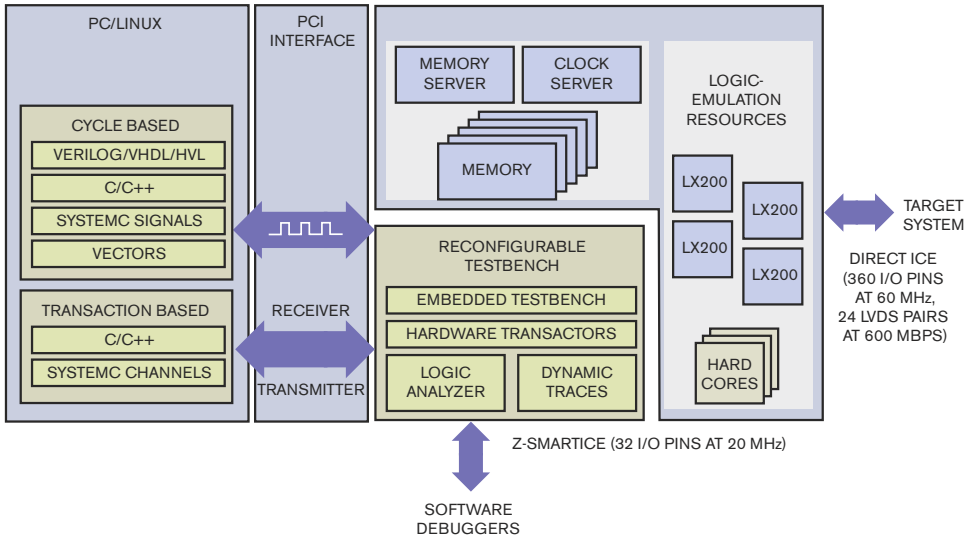


Figure 2 State-of-the-art emulator architecture supports IP evaluation, logic simulation, embedded-software debugging, and ICE functions and integrates seamlessly with traditional digital-logic simulators.

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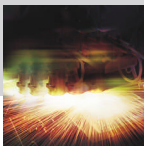

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of the core's functions. The possibility of plugging a core on an emulator board and quickly executing an evaluation using the architectural description of the rest of the system provides customers with the information they need. Meanwhile, the vendor decreases its marketing cost and increases the protection of its IP.

A quarter of a century ago, a design team would not develop software for a microprocessor without using its development system. Those systems were specific to each vendor and, in most cases, to one microprocessor. The primary advantage of an emulator is its flexibility. As **Figure 2** shows, designers can connect the development environment from ARM (www.arm.com), ARC (www.arc.com), or Tensilica (www.tensilica.com) to allow software engineers to debug their software in real time and model the rest of the system at various levels of abstraction. The feature allows true parallel development of hardware and software, enabling not only a shorter development cycle, but also early trade-offs between hardware and software implementations, thereby improving the overall quality of the product.

Using a workstation and an emulator such as Zebu-UF, the development team can tailor the instruction set of a configurable processor, such as the one from Tensilica, develop and debug the embedded software, and evaluate third-party IP. It can also debug the circuitry in an environment that allows the team to have constant access to the entire design regardless of the abstraction model of each block. The ability to use various abstraction levels for models enables engineers to as long as possible defer the final decision on the architecture of the product while they are developing and finalizing some of the blocks. They can simulate the entire system, including software, with acceptable throughput speed.

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The speed of compilation was one of the major drawbacks of early emulators. Compiling a design for emulation requires synthesis, partitioning, and a place-and-route tool (**Figure 3**). As the circuit grows, these functions grow at an increasing rate. If engineers had to wait hours between debugging runs, their productivity would suffer significantly. Emulator and hardware-accelerator vendors can now perform incremental circuit compilation so that they need to recompile only the changes while most of the circuit remains the same.

Early access to hardware implementations is especially important to embedded-software developers. Although embedded software depends on timing and interrupts, no ESL tool can support both. Traditional programming and modeling languages, such as C, C++, SystemC, and even Java, lack support for either time or interrupt mechanisms (**Reference 1**). As a result, software engineers cannot complete their work using logic simulators; they must rely on the actual hardware. Emulators provide the earliest support for real-time software debugging.

Architects can use TLMs of the rest of the system, whereas the emulator supports gate-level implementations of portions of the system. They can study the communication pattern between various blocks, refine the partitioning, and change the implementation of a function from hardware to software or vice versa to minimize bus traffic. The emulator imposes no restrictions on engineers concerning the modeling language they want to use to simulate the rest of the system.

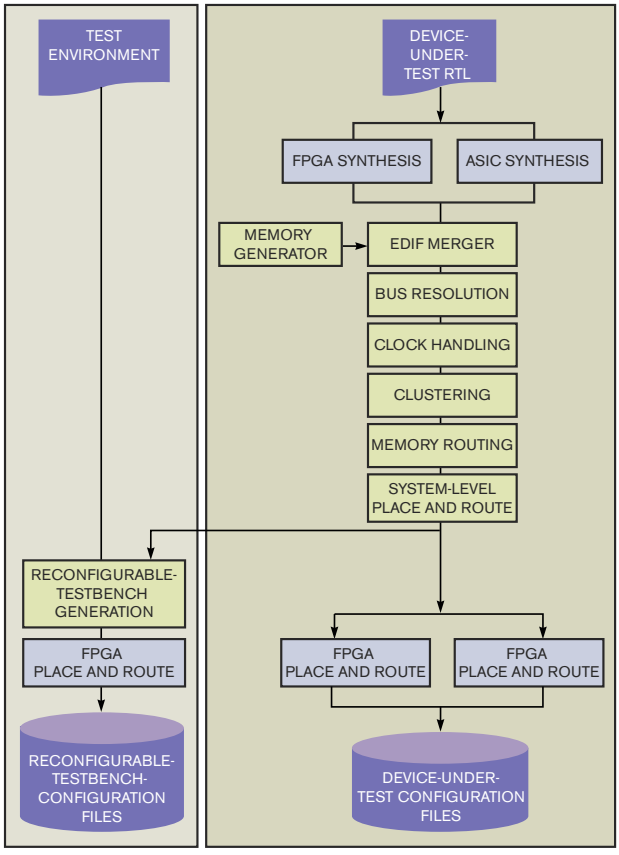


Figure 3 Engineers must map both the testbench and the design under test onto the emulator-hardware architecture. Vendors accelerate this time-consuming operation by using incremental compilation techniques.

Too often, engineers see the IC as the system. Yet, every IC must reside on a board, and engineers must now consider the effects of both the IC package and the board in determining the system's parameters. Designers can use an ICE (in-circuit emulator) and observe the behavior of the entire product, not just the IC, before releasing the design to a foundry. The ICE allows architects to simulate the entire product well before finalizing the design, thus increasing the chances of avoiding a redesign. Emulators, which engineers once used only for debugging at the last stages of design implementation and regression testing, are now becoming useful tools for system architects, as well. EDN

## REFERENCE

1 Lee, Edward E, "Absolutely Positively on Time: What Would It Take?" *IEEE Computer*, July 2005, pg 85.

## AUTHOR'S BIOGRAPHY

*Following a long career in engineering that culminated with his five-year stint as a technical editor at* EDN, *Gabe now runs GABEonEDA, a consulting company addressing communication and marketing issues in the EDA industry. You can reach him at gmoretti@gabeoneda.com.*

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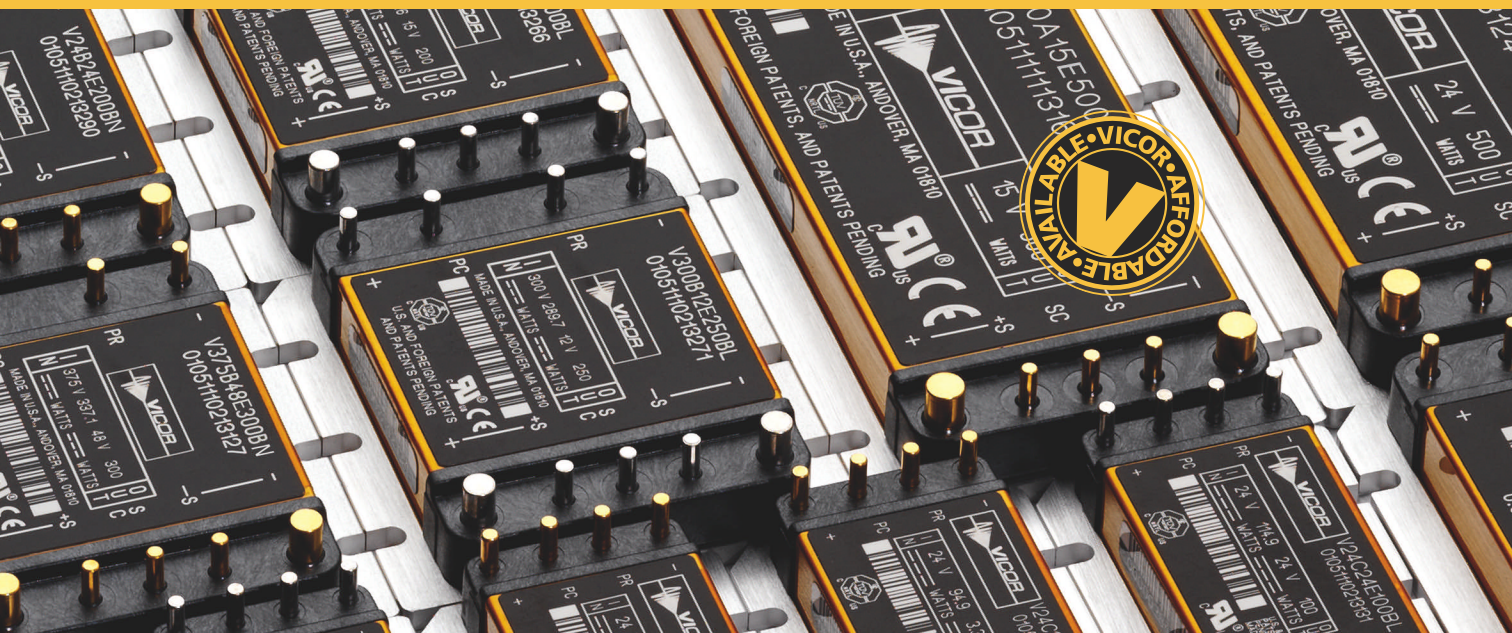

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# World's Fastest Triple Video ADC with Unmatched Color Accuracy

Intersil's ISL98001 offers sharp, clear images for HDTV, DVD, VCR, set-top box and PC monitor applications.

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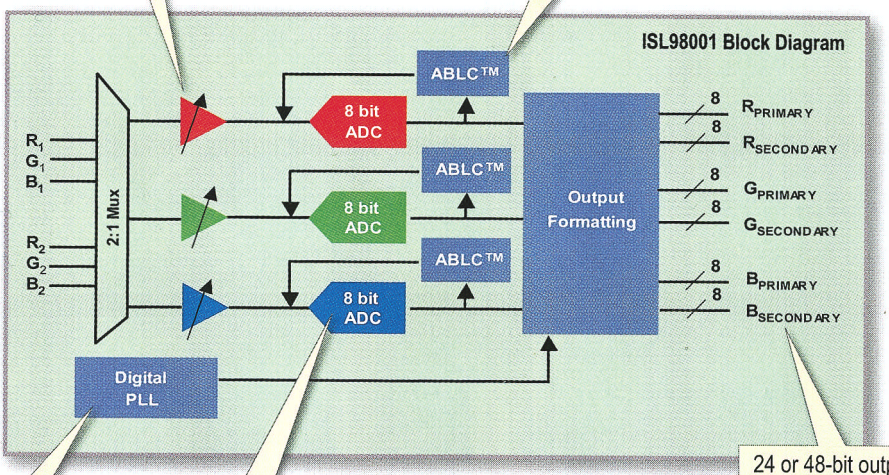
Gain control before the offset control, making adjustments independent.

Automatic Black Level Control continuously eliminates offset, ensuring all pictures have perfect black level and outstanding color matching.
**No user offset calibration required!**




- 250ps peak-to-peak jitter
- 64 sample phase choices
- 100% Macrovision® compliant

24 or 48-bit output modes support speeds up to 275Msps.

| SPEED GRADE | MAC PC MODE | MAX VIDEO MODE |
|---|---|---|
| ISL98001-140 | SXGA 75Hz | 720p/1080i |
| ISL98001-170 | UXGA 60Hz | 1080p |
| ISL98001-210 | WUXGA 60Hz | 1080p |
| ISL98001-240 | UXGA 85Hz | 1080p |
| ISL98001-275 | QXGA 60Hz | 1080p |

## Key Features

- 140MSPS, 170MSPS, 210MSPS, 240MSPS and 275MSPS maximum conversion rates
- Extremely fast recovery from VCR head switching
- Low PLL clock jitter for accuracy and stability

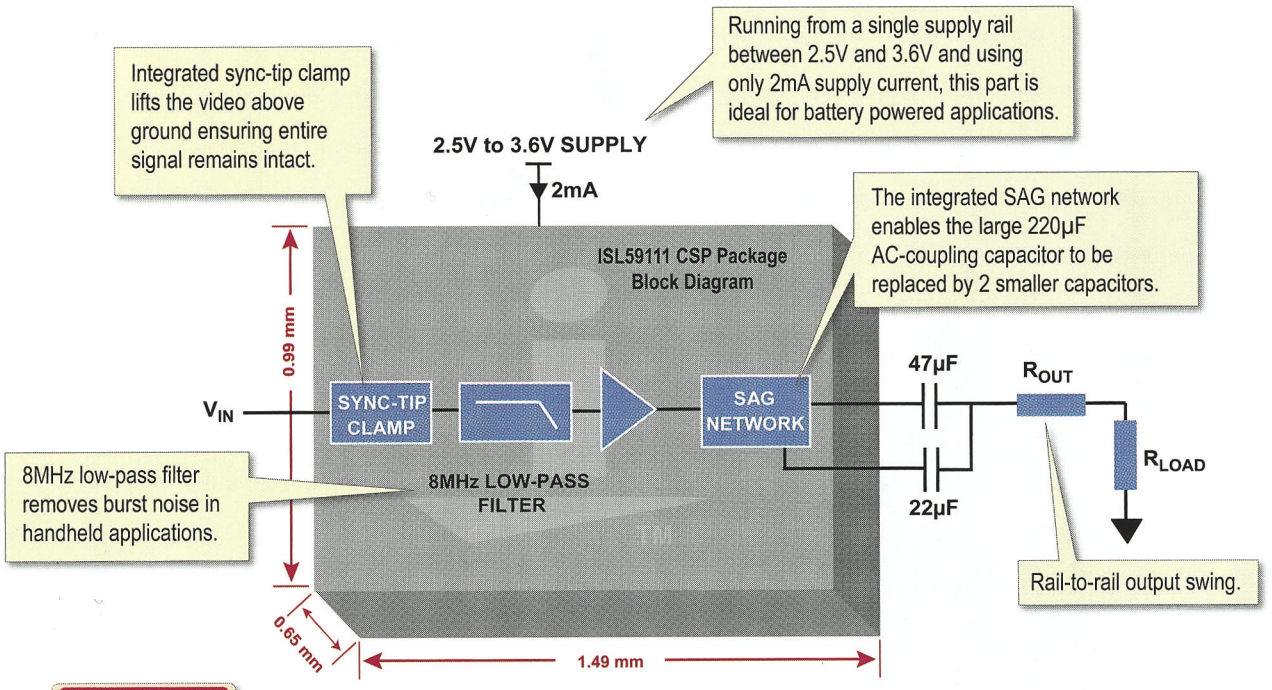
## Key Specifications

| Device | Resolution (bits) | Max Conversion Rate (MSPS) | Typical PLL Jitter (ps) (p-p) | Sample Phase Choices | Programmable Input Bandwidth (MHz) | CSYNC and SOG Support | Typical Power Dissipation @ Max Conversion Range (mW) | Package |
|---|---|---|---|---|---|---|---|---|
| ISL98001-140 | 8 | 140 | 250 | 64 | 100 to 780 | X | 950 | 128 Ld MQFP |
| ISL98001-170 | 8 | 170 | 250 | 64 | 100 to 780 | X | 1050 | 128 Ld MQFP |
| ISL98001-210 | 8 | 210 | 250 | 64 | 100 to 780 | X | 1100 | 128 Ld MQFP |
| ISL98001-240 | 8 | 240 | 250 | 64 | 100 to 780 | X | 1150 | 128 Ld MQFP |
| ISL98001-275 | 8 | 275 | 250 | 64 | 100 to 780 | X | 1200 | 128 Ld MQFP |

# Rail-to-Rail Amplification in the Tiniest of Packages

Available in Pb-Free Package

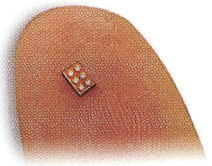
Minimal supply current requirements for battery-operated video met in a 1.5mm$^2$, 8MHz rail-to-rail composite driver.




## Key Features

- Shutdown current <2µA
- Minimal 2mA supply current reduces battery drain
- 2.5V to 3.6V supply rails
- 3-pole filter has -3dB roll-off at 8MHz
- Input signal DC restroration using a sync-tip clamp
- Faster power-down in 14ns
- Output current of 40mA to drive composite video
- Tiny, low-profile chipscale package. ISL59110 and ISL59112 available in SC-70 package.


6 Ld CSP



## Key Specifications

| Device | # of Amps | Slew Rate (V/µs) | $V_S$ (min) (V) | $V_S$ (max) (V) | $V_N$ (nV/√Hz) | BW @ -3dB (MHz) | Rail-to-Rail | Gain $A_V$ (min) (V) | $I_S$ (per amp) (mA) | $I_{BIAS}$ (µA) | $I_{OUT}$ (mA) | $V_{OUT}$ (V) | Diff Gain (%) | Diff Phase (°) | $V_{OS}$ (max) (mV) | $A_{VOL}$ or $A_{ZOL}$ (dB or V/mA) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISL59110 | 1 | 70 | 2.5 | 3.6 | N/A | 8 | YES | 2 | 2 | 5 | 40 | 3.2 | 0.1 | 0.05 | N/A | N/A | 6 Ld SC-70 T+R |
| ISL59111 | 1 | 70 | 2.5 | 3.6 | N/A | 8 | YES | 2 | 2 | 5 | 40 | 3.2 | 0.1 | 0.005 | N/A | N/A | 6 Ld CSP |
| ISL59112 | 1 | 85 | 2.5 | 3.6 | | 40 | YES | 2 (fixed) | 2 | 5 | 40 | 3.2 | 0.02 | 0.04 | N/A | N/A | 6 Ld SC-70 T+R |

# Smaller-Sized, Superior Protection in Dual-Protocol Transceivers from Intersil

Best-in-class components offering 15kV ESD protection in a space-saving QFN package option.

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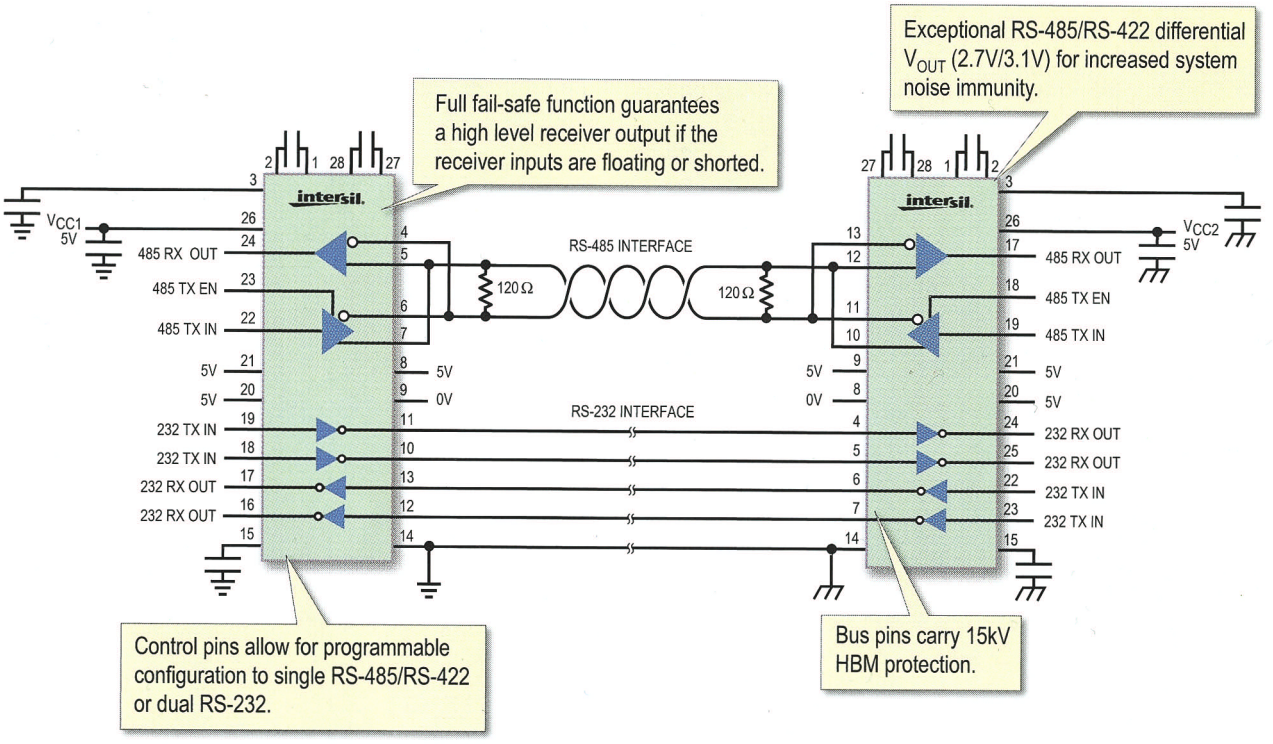
40 Ld QFN is 75% smaller than standard SOIC



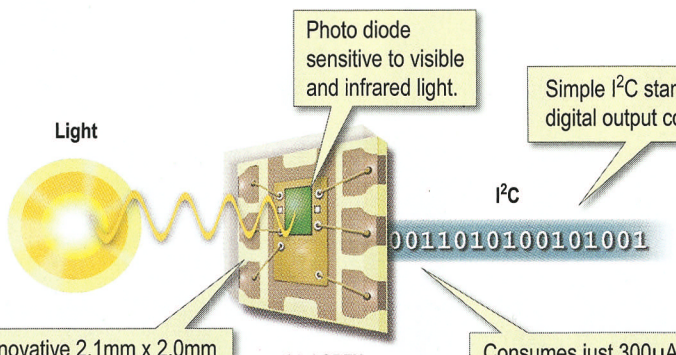

## Key Specifications

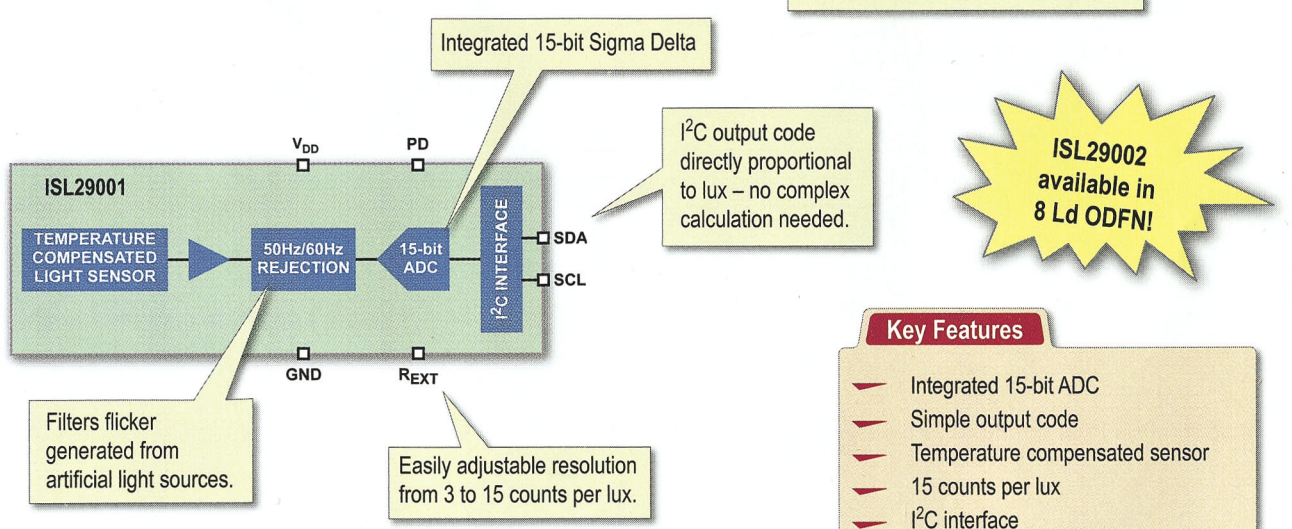
| Device | Supported Protocols | # of Ports | # of Tx/Rx per Port | High ESD (kV) | Data Rate RS-485/RS-232 (Mbps) | RS-485 Rx Fail-safe Type | $V_{LOGIC}$ Supply Pin? | RXEN Polarity | Loop-back Feature? | Operating $I_{CC}$ RS-485/RS-232 (mA) | SHDN $I_{CC}$ (µA) | $V_{CC}$ (V) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISL81387 | RS-232, RS-422, RS-485 | 1 | 1/1 RS-485, RS-422; 2/2 RS-232 | 15 | 20, 0.46/0.5 | Full | No | High | Yes | 1.6/3.7 | 30 | 5 | 20 Ld SOIC, 20 Ld SSOP |
| ISL41387 | RS-232, RS-422, RS-485 | 1 | 1/1 RS-485, RS-422; 2/2 RS-232 | 15 | 20, 0.46, 0.115/0.5 | Full | Yes | High and Low | Yes | 1.6/3.7 | 30 | 5 | 40 Ld QFN |
| ISL81334 | RS-232, RS-422, RS-485 | 2 | 1/1 RS-485, RS-422; 2/2 RS-232 | 15 | 20/0.5 | Full | No | None | Yes | 1.6/3.7 | 42 | 5 | 28 Ld SOIC, 28 Ld SSOP |
| ISL41334 | RS-232, RS-422, RS-485 | 2 | 1/1 RS-485, RS-422; 2/2 RS-232 | 15 | 20, 0.46, 0.115/0.5 | Full | Yes | Low | Yes | 1.6/3.7 | 80 | 5 | 40 Ld QFN |

# Intersil's New Light-to-Digital Converters Provide Pure 15-bit I²C Digital Data

Patterned upon the human eye, these integrated light sensors generate 15-bit effective resolution.

Available in Pb-Free Package




## Key Features

- Integrated 15-bit ADC
- Simple output code
- Temperature compensated sensor
- 15 counts per lux
- I²C interface
- 2.5V to 3.3V supply
- -40°C to +85°C temperature range

### Key Specifications

| Device | Peak Spectral Sensitivity (nm) | Supply Voltage (min) (V) | Supply Voltage (max) (V) | Supply Current (µA) | Lux Range (max) (Lux) | Counts per Lux (max) (Counts/ Lux) | Output Interface | Output Resolution (bits) | Integration Time (ms) | Package Dimensions (mm) | Pb-Free? | Enable Pin? | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISL29001 | 550 | 2.25 | 3.63 | 280 | 10,000 | 15 | I²C | 15 | 100 | 2x2.1x0.7 | Y | Y | 6 Ld ODFN |
| ISL29002 | 550 | 2.25 | 3.63 | 400 | 50,000 | 15 | I²C | 15 | 100 | 3x3x0.7 | Y | Software Enabled | 8 Ld ODFN |

# 4.5V to 28V Wide $V_{IN}$ and Adjustable Operating Frequency Offers Design Flexibility and Ease in General Purpose Applications

ISL6420A wide $V_{IN}$ Step Down controller combines control, output adjustment, monitoring and device protection in a single component.

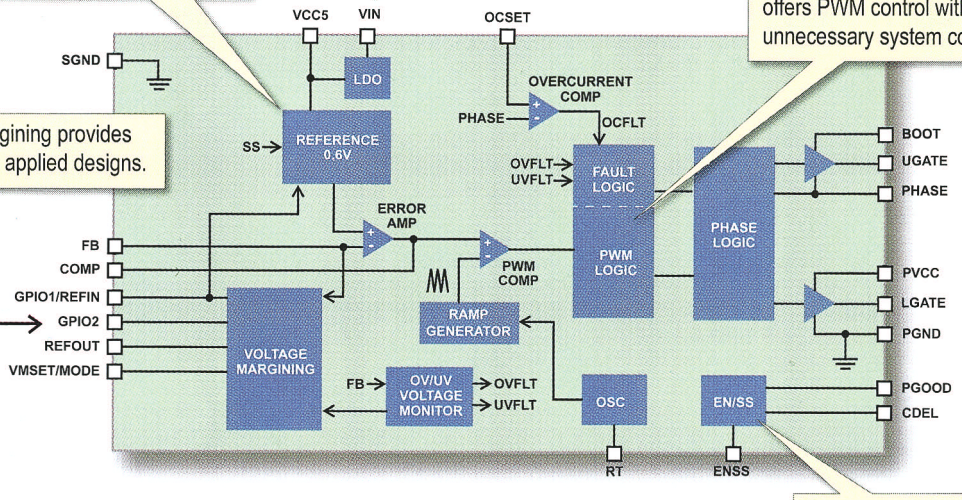
Available in Pb-Free Package

Excellent output voltage regulation (0.6V internal reference; ±1.0% RAOLT) provides unmatched stability throughout.

Broad voltage input range (4.5V to 28V) offers flexibility and use in a variety of applications.

Simple single-loop control design offers PWM control without unnecessary system complexity.

Output voltage margining provides added safety to the applied designs.




Programmable soft-start available through EN/SS pin capacitor value setting.

## Key Features

- Operates on a 4.5V to 28V input range
- Diode emulation during start-up for pre-biased load applications
- Adjustable operating frequency from 100kHz to 1.4MHz offering potential cost and space savings
- Programmable soft-start available through EN/SS pin capacitor value setting
- Voltage margining protects your design

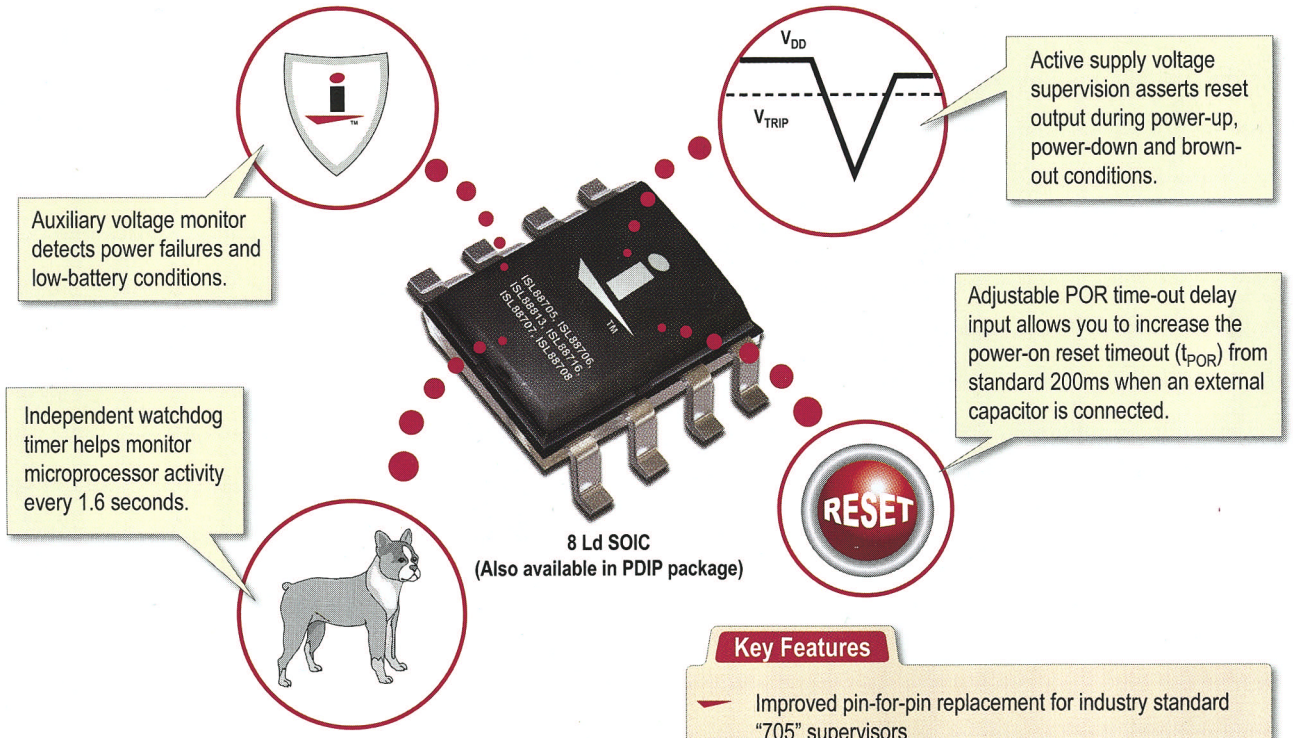
## Key Specifications

| Device | Device Description | $V_{IN}$ (min) (V) | $V_{IN}$ (max) (V) | $V_{OUT}$ (min) (V) | $V_{OUT}$ (max) (V) | $I_{OUT}$ (max) (A) | $V_{BIAS}$ (V) | $I_{CC}$ (min) (mA) | $I_{CC}$ (typ) (mA) | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| ISL6420A | PWM Controller with Wide $V_{IN}$, Start-Up into Pre-Bias Load | 4.5 | 28 | 0.6 | $V_{IN}$-0.5V | 20 | 5 | 1.4 | 2 | 20 Ld QFN, 20 Ld QSOP |
| ISL6420 | Advanced Single Synchronous Buck Pulse-Width Modulation (PWM) Controller | 4.5 | 16 | 0.6 | $V_{IN}$-0.5V | 20 | 5 | 1.4 | 2 | 20 Ld QFN, 20 Ld QSOP |

# Multi-Function Integration Excellence in a Power Supervisor Saves Cost and Frees Board Space

Protect your system and improve reliability with the ISL887XX/813 family.

Available in Pb-Free Package




## Key Features

- Improved pin-for-pin replacement for industry standard "705" supervisors
- Ultra-low 10µA supply current
- ±1.8% voltage trip point accuracy
- Added time-out adjustability on POR is an industry first for voltage supervisors

## Key Specifications

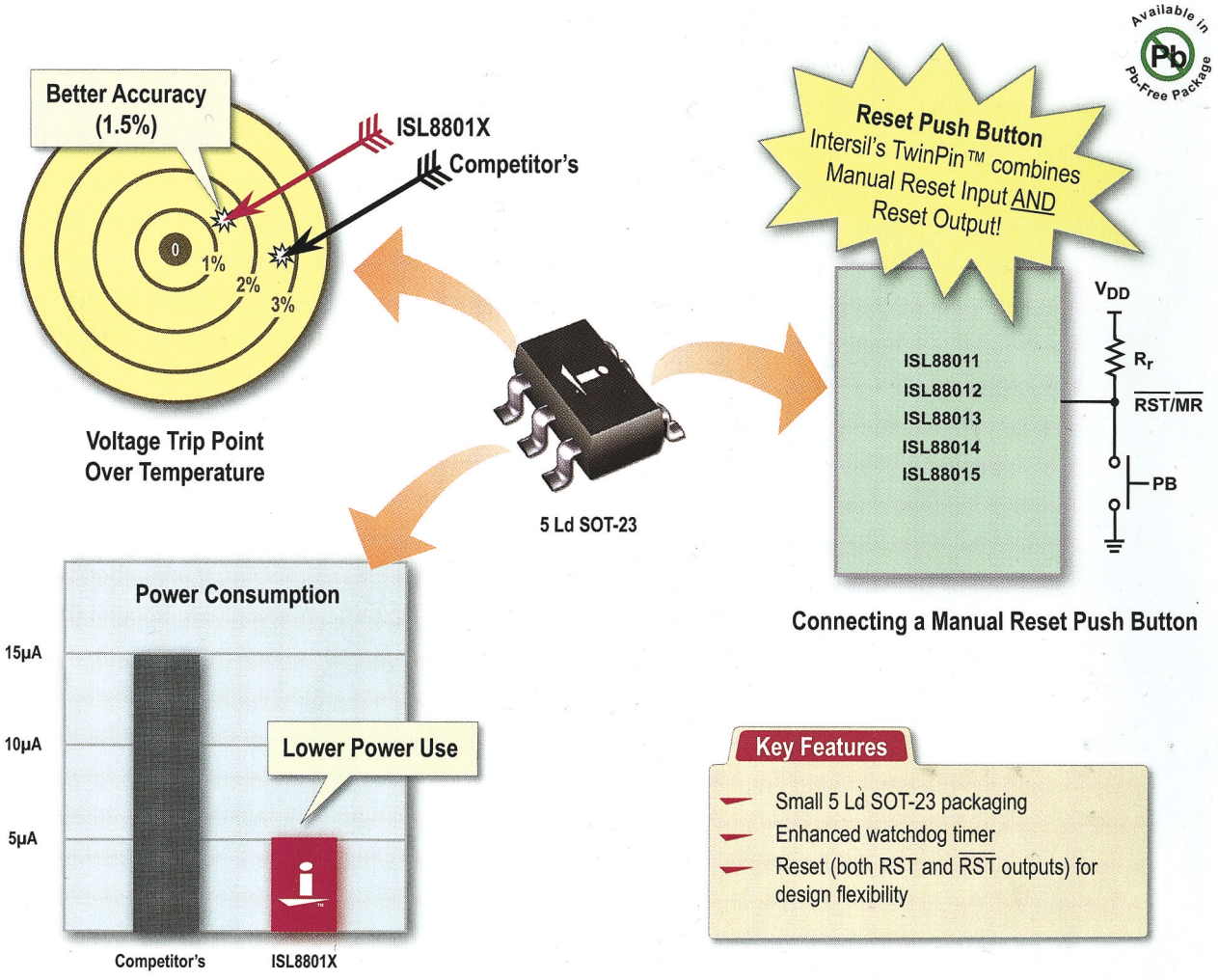
| Device | Number of Voltage Monitors | Fixed $V_{TRIP}$ | Adj. $V_{TRIP}$ (Resistors) | Open-Drain $\overline{RST}$ | Push-Pull RST | Manual Reset | WDI/WDO | Adj. POR Timeout | Package |
|---|---|---|---|---|---|---|---|---|---|
| ISL88705 | 2 | Y | Y | Y | | Y | Y | | 8 Ld PDIP, 8 Ld SOIC |
| ISL88706 | 2 | Y | Y | Y | | Y | Y | | 8 Ld PDIP, 8 Ld SOIC |
| ISL88707 | 2 | Y | Y | Y | Y | Y | | Y | 8 Ld PDIP, 8 Ld SOIC |
| ISL88708 | 2 | Y | Y | Y | Y | Y | | Y | 8 Ld PDIP, 8 Ld SOIC |
| ISL88813 | 2 | Y | Y | | Y | Y | Y | | 8 Ld PDIP, 8 Ld SOIC |
| ISL88716 | 2 | Y | Y | | Y | Y | Y | | 8 Ld PDIP, 8 Ld SOIC |

# Intersil Voltage Supervisors

High Performance Analog

# Get High-Precision Accuracy with Low Power Consumption

The ISL8801X family provides improved voltage monitoring accuracy with low power and a host of other key features.




## Key Features

- Small 5 Ld SOT-23 packaging
- Enhanced watchdog timer
- Reset (both RST and $\overline{RST}$ outputs) for design flexibility

## Key Specifications

| Device | Number of Voltage Monitors | Fixed $V_{TRIP}$ | Adj. $V_{TRIP}$ (Resistors) | Open-Drain RST | Push-Pull RST | Push-Pull RST | TwinPin™ MR/RST | Enhanced WDT | Adj. POR Timeout | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| ISL88011 | 1 | Y | | Y | Y | Y | Y | | Y | 5 Ld SOT-23 |
| ISL88012 | 2 | Y | Y | Y | Y | Y | Y | | | 5 Ld SOT-23 |
| ISL88013 | 1 | Y | | Y | Y | Y | Y | Y | | 5 Ld SOT-23 |
| ISL88014 | 1 | | Y | Y | | | Y | | Y | 5 Ld SOT-23 |
| ISL88015 | 1 | | Y | Y | | | Y | Y | | 5 Ld SOT-23 |

BY ARUN KOTTOLLI • OPEN-SILICON

# The economics of structured- and standard-cell-ASIC designs

STRUCTURED ASICs OFFER COST AND PERFORMANCE THAT FALL BETWEEN FPGAs AND TRADITIONAL STANDARD-CELL ASICs. BUT THEIR INTRODUCTION HAS COMPLICATED THE CHOICE OF THE RIGHT SILICON.

Although structured ASICs promise a shorter schedule than standard-cell ASICs, this abbreviation comes at a price. Structured ASICs are more expensive on a per-unit basis, allow less customization, and offer lower performance than standard-cell ASICs. For various designs, customers often have to choose from standard-cell ASICs, structured ASICs, and FPGAs.

To select the right ASIC, you could use a three-step approach. The first step would be to look at the technical requirements and feasibility of the design for structured-ASIC and standard-cell-ASIC technologies. Next, you would perform a financial analysis. Finally, you would employ a financial model that looks at the total time value of money and the NPV (net present value) of the ASIC project.

## BASIC ASIC PRICING

ASIC pricing is usually complex and depends strongly on the customer's projected volume. However, the fundamental cost aspects of an ASIC design do not change. You can break up the cost of any ASIC into two basic components: a fixed NRE (nonrecurring-engineering) charge and unit pricing. ASIC vendors charge a fixed NRE to cover the expenses they incur for physical design—from handoff to tape-out. NRE charges include costs for IP (intellectual property), masks, package design, test development, debugging, and hardware. The design-engineering costs include engineering efforts, EDA tools, and hardware. The IP-licensing fee is a one-time cost you pay to the IP vendor for third-party IP. Some companies pass these charges on to their customers. In the case of FPGAs and structured ASICs, manufacturers do not customize the package, test cost, and die for each project; thus, they achieve a lower NRE cost but may require a trade-off in flexibility.

Meanwhile, the industry bases unit pricing or cost on volume shipments. Die size, packaging type, per-part royalty, and testing costs incurred on every part primarily drive unit cost. For standard-cell ASICs, the components of chip COG (cost of goods) may be transparent to the fabless-chip customer or the system house; manufacturers base the pricing of FPGAs and structured ASICs on the value of the parts.

Unit cost varies with the number of parts that customers order, and silicon vendors commonly offer volume discounts. Larger orders reduce the percentage of overhead in the chip cost per unit, which allows fabless-chip customers or system houses to get reduced pricing for volume purchases. Additionally, unit cost may improve over time due to improved manufacturing efficiencies, yield enhancements, and better yield management.

Developing an ASIC from its architectural specifications breaks into three steps: architecture to RTL or netlist, RTL or netlist to tape-out, and tape-out to volume production or RTP (release to production, **Figure 1**). Development of the chip architecture and the associated RTL or netlist is primarily the ASIC customer's responsibility. ASIC vendors normally do not take ownership for developing the architecture or associated RTL of a design. The ASIC vendor takes either the RTL or a netlist as the customer deliverable and is responsible for producing the prototypes, testing the prototypes, and characterizing and qualifying the product for volume production. The ASIC vendor then delivers tested working parts to the customer.

## ARCHITECTURE TO RTL OR NETLIST

Customers often provide RTL or a netlist to the ASIC vendor. Converting architectural specifications into RTL or a netlist primarily involves defining the microarchitecture, writing RTL code, developing a functional verification for the RTL description, and synthesizing the gate-level netlist. The schedule for this process varies with design complexity and can range from months to more than a year. More than 60% of this time involves functional verification. For complex SOC (system-on-chip) designs, functional verification can consume more than 70% of the total design schedule.

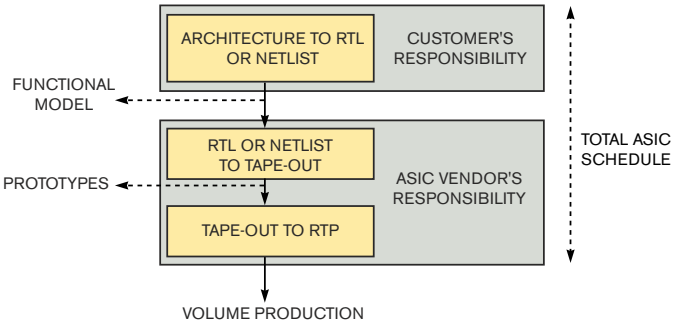



Figure 1 The development of an ASIC from its architectural specifications breaks down into three distinct steps.

RTL or netlist to tape-out constitutes the physical-design process. This process comprises synthesis, DFT (design for test), floorplanning, timing analysis, clock insertion, place and route, timing closure, reliability analysis, and physical-design verification. For FPGAs and structured ASICs, in which manufacturers lay out cells with built-in DFT, physical design implies routing the top metal layers, reliability analysis, and timing closure, which results in less time for physical design. A chip from a standard-cell implementation typically has better performance and a smaller die for the same level of complexity than an FPGA or a structured-ASIC implementation.

Once you tape out a design for a standard-cell ASIC, it takes about four to eight weeks to process a more-than-30-layer design and provide prototypes to the customer. For structured ASICs, the base wafer is processed; therefore, only the upper-level-metal and via layers require processing. Using a structured ASIC results in substantial time savings, with parts available for delivery in just a few weeks. After initial prototypes are available, they must undergo the RTP phase, requiring testing, qualification, and characterization, and designers must analyze and optimize the production process for maximum yield before the part enters full production.

The time it takes for a prototype to begin volume production varies from 12 to 26 weeks for a standard-cell ASIC. Structured ASICs require about six to eight weeks, because they need no detailed characterization, process qualification, and yield optimization. In parallel with the ASIC-RTP process, the customer must perform functional verification and develop and verify the software that will run on the silicon. This process may take longer than the RTP approach and could delay the volume-production shipment of parts.

In production, the time it takes to fill a customer's order is typically the same for standard-cell ASICs and structured ASICs for the same number of process layers, because the wafers require processing from scratch, and they also require packaging and testing. Therefore, neither process offers a great advantage over the other.

## A NOTE ABOUT NPV

**You calculate NPV (net present value) by discounting all the cash outflows at the hurdle rate of the customer's company. Companies internally set the hurdle rate, and it can vary substantially from project to project, depending on risk factors and prevailing interest rates.**

## COST STRUCTURE

Manufacturers custom-design each ASIC program for standard-cell ASICs, and the NRE charges are usually higher than for a structured ASIC or an FPGA. Custom design implies that every chip goes through physical design with cell placement and routing of all metal layers. This approach is time-consuming, and it results in longer schedules and higher costs for the engineering efforts and tools. The layout of the logic cells provides maximum performance in a minimum area, which results in a smaller die and, hence, a lower unit cost.

Going to a standard-cell ASIC can impact a schedule for as long as 18 months. The financial analysis accounts for the lost sales during this period as "lost-opportunity costs." The longer time is mainly due to the need for the detailed layout design, complete manufacturing processes, and release to production.

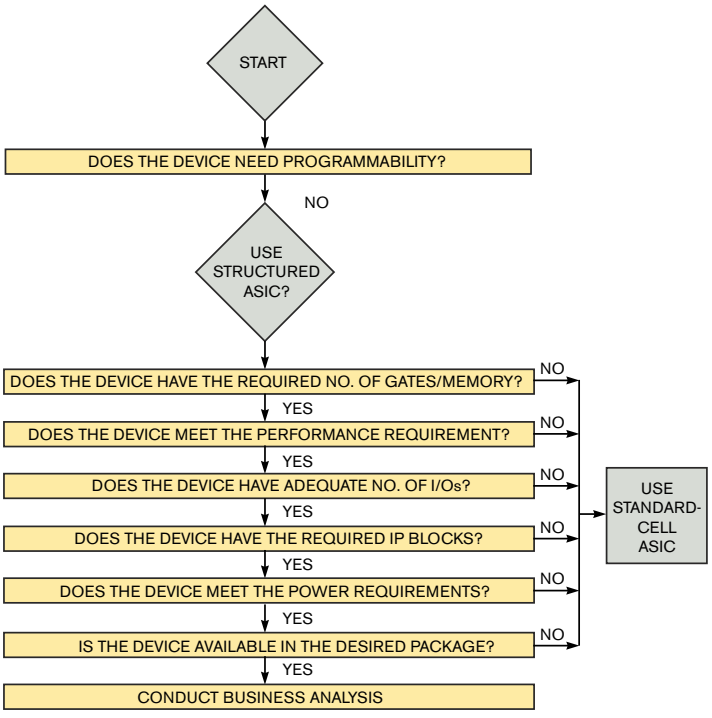



Figure 2 You can systematically carry out the technical feasibility of implementing the design in a standard-cell or structured ASIC by carefully identifying the needs and mapping those needs to the appropriate ASIC option.

The biggest advantage of standard-cell ASICs is that they offer the lowest unit cost, because their custom design results in a smaller die. Better package selection and testing also lower the unit cost. In a high-volume market, cost savings on a per-unit basis lead to significant market advantages. Additionally, you can use smaller packages and similarly sized structured ASICs, resulting in smaller pc-board form factors. Furthermore, customers get added flexibility and higher performance from both speed and power perspectives.

The lower unit cost compensates for the overall higher upfront NRE costs and the impact on the schedule. Therefore, you need to consider the total cost of the project over the life span of the ASIC. NRE cost with a structured ASIC is usually lower than with a standard-cell ASIC, mainly due to predesigned cell layout, fixed IP, standard packaging, and minimum routing at the top metal layers. Cell layout and cell-level routing are standard, so new designs require minimal effort. The manufacturing NRE cost is also lower, because the wafers are partially processed, and multiple customers share them. For a new design, only the top metal-layer masks require processing; hence, mask costs are lower. The packaging for each chip is standard, leading to economies of scale and reducing the package's NRE cost. The limitation of this platform, however, is that the design must fit the available prepackaged structured-ASIC IP, gates, and memory configurations.

Structured ASICs allow a quick turnaround from RTL to

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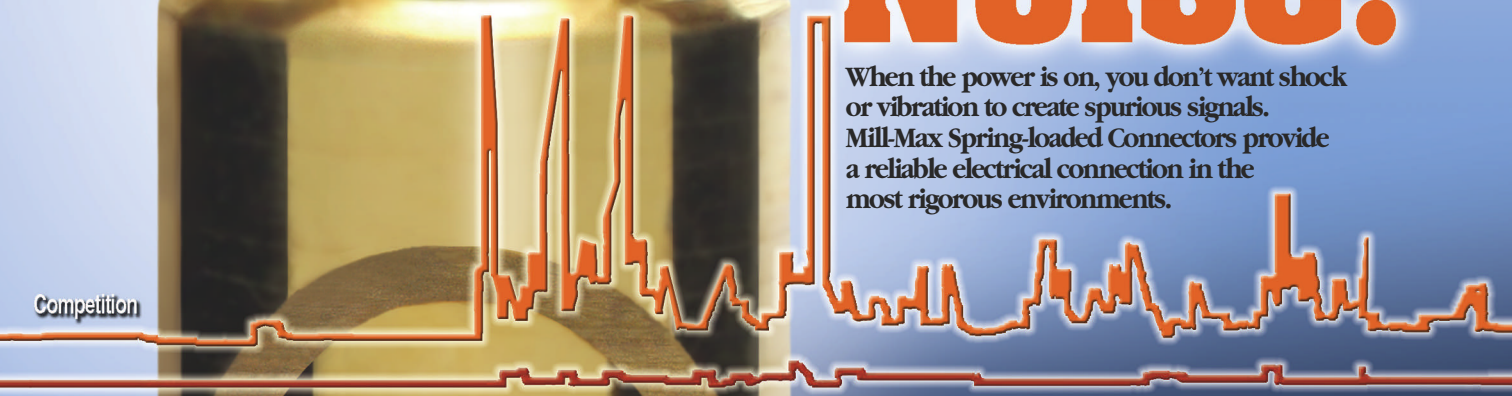


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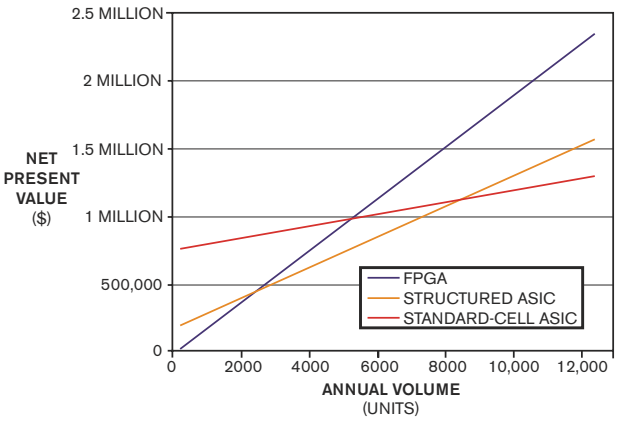


Figure 3 At volumes of less than 1500 parts per year, such as might be the case for an avionics-control chip, an FPGA may be your best bet.

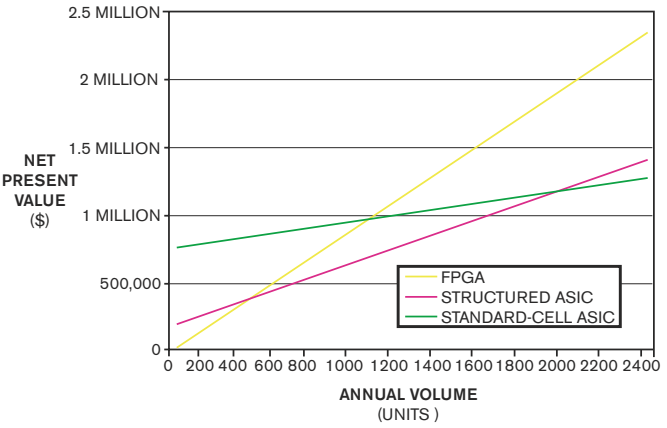


Figure 4 An NPV analysis shows that, even at volumes of 2200 parts per year, a standard-cell ASIC is the least costly alternative.

parts. The physical-design-cycle time is low because only the top metal layers require routing, the package is standard, and the wafers are partially processed and stored as inventory. This approach allows a shorter turnaround time in both the design and the manufacturing phases.

Unit costs for a structured ASIC are higher than those for comparable standard-cell ASICs, primarily due to fixed-cell layout, which results in less cell usage, higher routing overheads, and increased use of silicon area for the design. A larger die directly impacts the unit cost. The use of suboptimal packaging further increases the unit cost. Generic packaging typically has a larger form factor and increases overall product and system costs. Test costs may also follow a similar cost increase over standard-cell ASICs.

Selecting the best silicon option for a given design is always a challenge. The best way to make this decision is to start with a technical-feasibility study to determine whether an FPGA, structured-ASIC, or standard-cell-ASIC platform meets the design requirements. If more than one silicon approach is technically feasible, a financial analysis can determine the optimal choice.

The best option is the one that offers the lowest cost or the highest returns. For a system manufacturer, the lowest cost for an ASIC is important because it is easy to determine and it directly affects the cost of the final product. You can attribute the highest returns from selling the final system to several factors, including market requirements, the ASIC platform, software, and market conditions. It often becomes difficult for a company that sells complete systems to gauge the returns from the ASIC.

## TECHNICAL-FEASIBILITY STUDY

You can calculate the technical feasibility of implementing the design in a standard-cell or structured ASIC by carefully identifying the design needs and mapping those needs to the appropriate ASIC option (**Figure 2**). Often, a design needs complex IP, such as analog/mixed-signal blocks. Nonavailability of such IP may prevent the use of a structured ASIC. Alternatively, in some cases, the IP is available, but its performance is unacceptable for the design. For example, the CPU available in the structured ASIC may run at a maximum frequency of 250 MHz, even though the design calls for a CPU running at 400 MHz.

If the standard-cell ASIC is the only option available, then the decision is clear. Often, a combination of structured-ASIC and discrete components may also meet design requirements. Under such conditions, you must conduct a business analysis to identify the best option that offers the lowest cost.

## BUSINESS ANALYSIS

If the design is feasible for an FPGA, structured ASIC, or standard-cell ASIC, then you should base your final decision on cost. You can do your financial analysis by calculating the NPV of all the options (see **sidebar** "A note about NPV"). The ASIC option with the lowest cost at the projected volume is your best choice. For NPV analysis, you must select a suitable discount rate.

The following case studies use a discount rate of 8.5% for NPV analysis. Varying the discount rate does not affect the final outcome of the analysis because the studies discount all the costs at a uniform rate. For a business analysis, you need to know the volume or number of ASICs needed per year, the projected life span of the ASIC, and the total NRE charges for that ASIC option.

The NRE figures in the case studies include only charges that projects incur after the netlist stage and before the initial prototypes. NRE charges you incur during architecture and RTL design are common for all types of ASICs; therefore, this comparative analysis does not take them into account. For the case studies, assume that you can implement the design in both a structured and a standard-cell ASIC. The goal of these studies is to determine the cost of all the possible ASIC options.

## CASE STUDIES

In one case study, assume that an ASIC has 250,000 gates running at 200 MHz and requires implementation in a 250-pin BGA package. For a structured ASIC, the average NRE charges are $200,000, and unit cost is around $40. Standard-cell ASICs have an NRE cost of approximately $800,000, and the unit cost is around $12. For an FPGA, assume NRE costs of zero and unit costs of around $80. Assume an ASIC life cycle of three to five years.

Conducting an NPV analysis for various volumes over a range of projected annual number of parts for five years gives you the total cost of the silicon option for each of the projected volumes. Because all the financial transactions in the procurement of the

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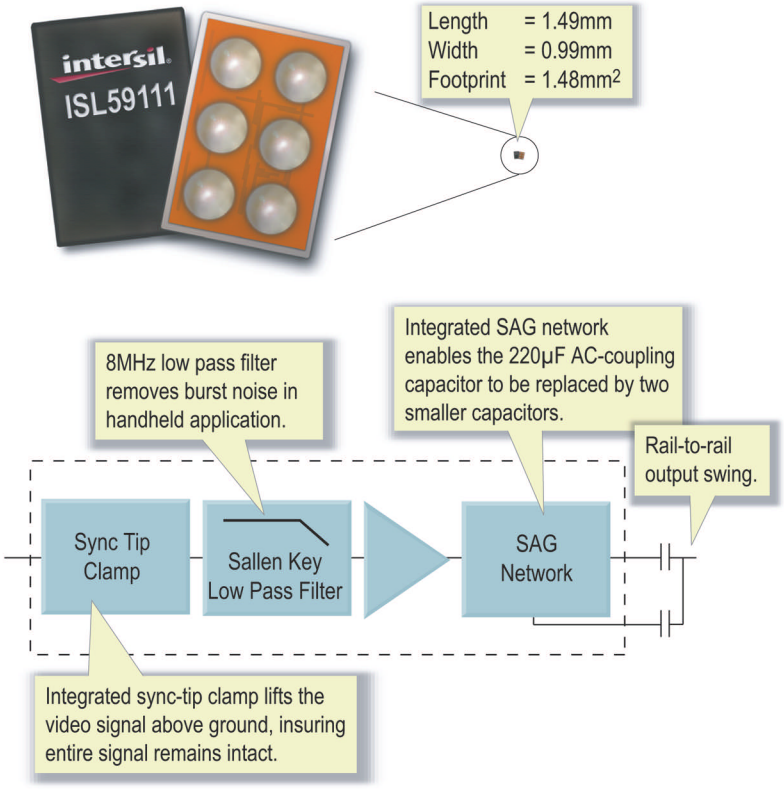


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ASIC are cash outflows, the numbers are positive for the NPV calculation. The analysis considers the ASIC option with the lowest NPV as the most suitable approach.

**Table 1** on the Web version of this article at www.edn.com/ms4178 compares the total costs of FPGAs, structured ASICs, and standard-cell ASICs for the projected volume. **Figure 3** helps clarify the data in the **table** by depicting how the NPV of various ASIC options changes with volumes.

**Figure 3** and **Table 1** show that, for volumes of less than 1500 parts per year, such as for an avionics-control chip—an FPGA may be your best bet. If the product has a demand of more than 2000 but less than 8500 parts per year, such as for a low-volume communication base station, a structured ASIC offers the lowest NPV and, hence, is the best option. If the annual demand increases to more than 8500 parts, a standard-cell ASIC is the right choice. In systems such as cell phones or LCD controllers, which have high annual volumes and are price-sensitive, a standard-cell ASIC is best.

You can run a similar analysis for ASICs with different unit costs and with different NRE charges, but the conclusion is the same. FPGAs are best for low volumes; at slightly higher volumes, structured ASICs offer the lowest cost; and at high volumes, a standard-cell ASIC is the ideal approach. Choosing an ASIC depends on having a good projection of the product's volume shipments and the unit cost of the ASIC.

In another case study, consider a complex system design with 5 million gates, 3 Mbits of internal memory, and a high-speed SERDES (serializer/deserializer) interface. Using a structured ASIC, the average NRE cost for such a chip is $250,000, and unit cost is $120. A standard-cell ASIC has an NRE cost of $1 million and a unit cost of $30. For an FPGA-based option using multiple FPGAs, the NRE cost is almost zero, and the total unit cost is around $240.

Conducting an NPV analysis for the above case and plotting the NPV for various annual unit volumes for each option show that, even at volumes of 2200 parts per year, a standard-cell ASIC offers the least costly option (**Figure 4**). If you use the ASIC for enterprise routers or digital set-top boxes, which have large annual volumes, a standard-cell ASIC is the best approach. If the application of the ASIC is in industrial measuring or control devices, which have moderate or unpredictable volume shipments, a structured ASIC is a better choice.

These two examples show that, at higher design complexities, a standard-cell ASIC offers a less costly ASIC approach, even at lower volumes. The advantage of having a low unit cost outweighs the higher NRE costs associated with a standard-cell implementation. Both an FPGA and a structured ASIC may offer lower initial costs and shorter times to market at high overall costs.

In a third case study, a high-end ASIC may contain 12 million to 20 million gates and 10 to 20 Mbits of memory along with multiple SERDES interfaces and a high-speed DDR interface. You can implement this design in a 250- to 400-sq-mm die in a flip-chip package, but you cannot implement the same design in a single FPGA or structured ASIC. However, you can implement the entire design in multiple FPGAs or structured ASICs.

Assume that this ASIC costs about $150 to $320 per part with an NRE charge of approximately $2 million to $2.5 million. If you were to implement the same design in multiple structured ASICs, the NRE charges would be around $750,000 with a unit cost of $1000. You could implement the design with multiple FPGAs and other discrete chips; then, the total cost for each design would be approximately $4000. A common industry perception is that, for high-end designs, standard-cell ASICs are expensive and need high volumes to justify their costs. NPV analyses bring out interesting results (**Figure 5** and also **Table 2** on the Web version of this article at www.edn.com/ms4178).

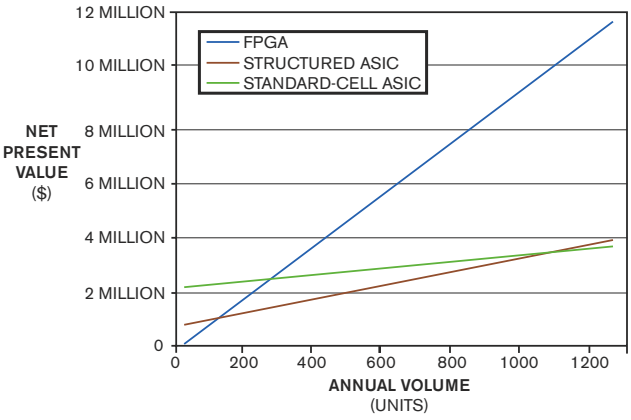


Figure 5 For high-end ASIC designs, a standard-cell ASIC makes economic sense only when volumes exceed 1200 per year.

The NPV analysis clearly shows that, in the case of a high-end ASIC design, a standard-cell ASIC makes economic sense only when volumes exceed 1200 per year. At volumes lower than 1200, a structured ASIC may make economic sense. However, for annual volumes of less than 100, an FPGA is the best choice. Designers should implement high-end telecom devices, such as ISP (Internet-service-provider) routers, which have annual volumes of less than 100 units per year, in FPGAs or structured ASICs. On the other hand, if you expect the product to sell in large volumes, such as server chip sets, a standard-cell ASIC has the lowest cost.

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Selecting an ASIC involves technical-feasibility and business analyses. Often, the technical-feasibility analysis can determine the type of ASIC. A structured ASIC has severe technical limitations compared with a standard-cell ASIC. If you can implement the design in both a structured ASIC and a standard-cell ASIC, you should perform an NPV analysis to determine the optimal ASIC. To conduct an NPV analysis, you need to know the NRE charges, unit cost, annual product volumes, and discount rate. The results show that, for a chip that you can technically design as a standard-cell ASIC or a structured ASIC, the application segment and the anticipated volume requirements primarily determine your choice. EDN

## AUTHOR'S BIOGRAPHY

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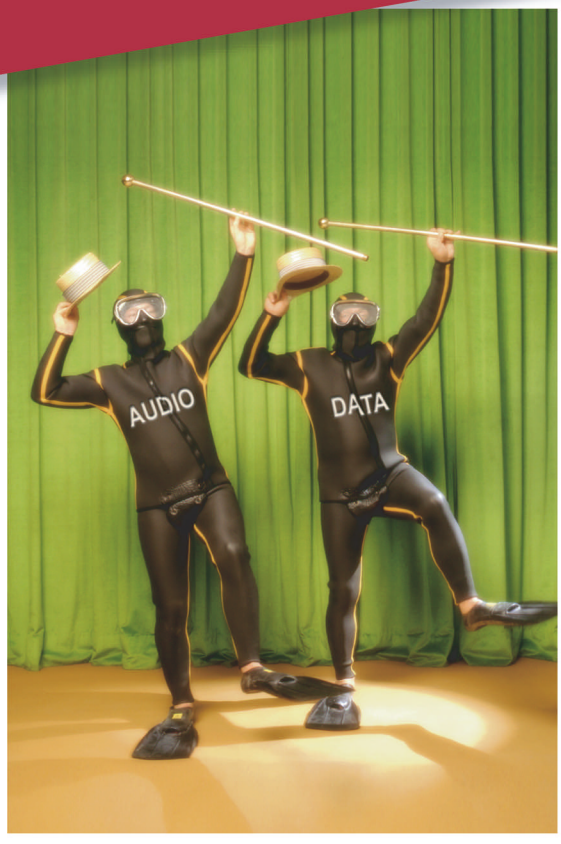


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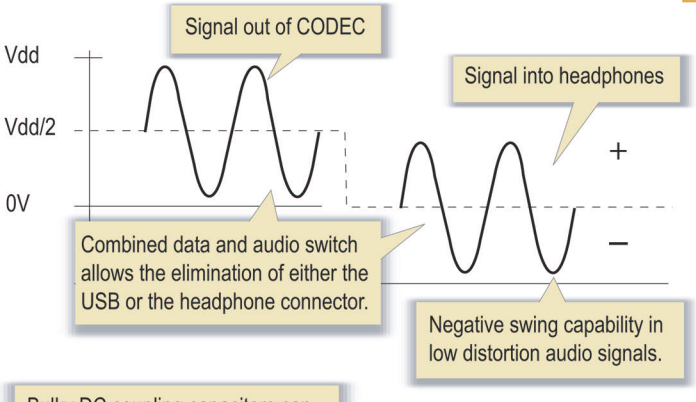


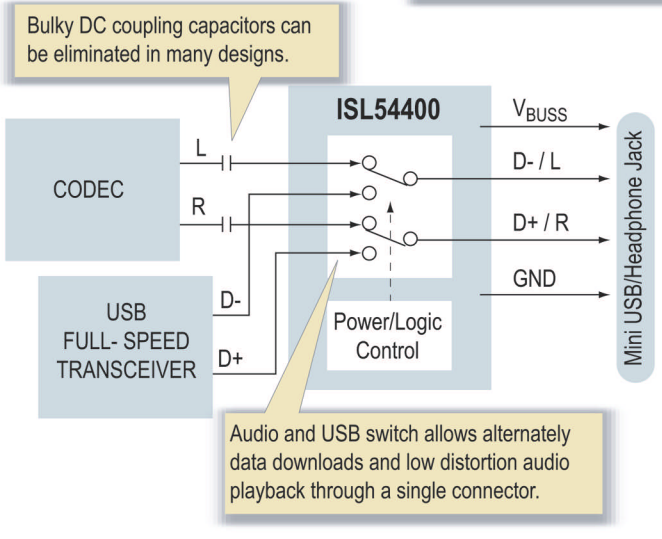


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# Mobile applications challenge test-and-measurement tools

ADVANCES IN PROBING AND TRIGGERING AND IN SIMULTANEOUSLY MONITORING MULTIPLE BUSES—INCLUDING HIGH-SPEED SERIAL BUSES—ARE ADAPTING LOGIC ANALYZERS TO THE WORLD OF FAST, LOW-POWER MOBILE APPLICATIONS.

Mobile technology is clearly a force in the market. Laptop-PC sales have overtaken those of desktops. Compact multimedia devices ranging from DVRs (digital video recorders) to set-top boxes and gaming platforms are now in millions of homes. The Pentium M from Intel (www.intel.com), Cell technology from Sony (www.sony.net) and IBM (www.ibm.com/chips), and, in the future, Uniphier from Matsushita (www.panasonic.co.jp/semicon/e-index.html) exemplify the powerful silicon components that are fueling the mobile revolution. Demand for mobile processors such as these, and the end products that use them, makes minimizing time to market an urgent priority.

When designing for mobility, designers must take some unique issues into account. These issues include space constraints due to product miniaturization and the increasing use of low-amplitude/low-power signals to preserve battery life. Mobile products are under constant pressure to deliver more features and more performance, with longer battery life in smaller form factors. Designers are looking for measurement approaches to help them evaluate, validate, and troubleshoot emerging mobile products under crushing time pressure. These approaches must provide state-of-the-art performance and adapt to the special requirements of the mobile platform.

In some functional respects, a measurement or a debugging task on a mobile platform is similar to its desktop counterpart. For examining CPU and bus events, the preferred measurement tool is the logic analyzer. It is the only tool that can acquire the full width of a data stream, map it into a comprehensible format, and display time-correlated results as a binary timing diagram or as a series of states expressed in hexadecimal form. In addition, disassembly tools are available to map the code to even higher level mnemonics. The same logic analyzer serves all digital-acquisition needs, including those of compact and mobile products.

But mobile platforms present a special challenge. They often require the measurement tool to adapt to a cramped, delicate environment that makes difficult demands on the hardware, particularly in regard to signal probing. Designers of mobile platforms can simplify their future troubleshooting work by paying attention to KOVs (keep-out volumes) and the requirements of interposers and midbus probes. The term "KOV" is a simple expression with complex implications for probe design. In the context of practical measurement tools, KOV dictates the allowable size of a probe. Component manufacturers handed down the KOV as a specification to ensure that their sockets have a physical buffer zone or clearance around them. This clearance area guarantees that designers can easily install and remove the device and its heat sink.

A by-product of the KOV guideline is its effect on the size of logic-analyzer probes, which must be small enough to fit the device-under-test socket without violating the KOV. In effect, the entire probe front end must be as small as or smaller than the device itself. The KOV is a defining specification for interposer probes.

Interposer probes typically fit into a socket or a connector to

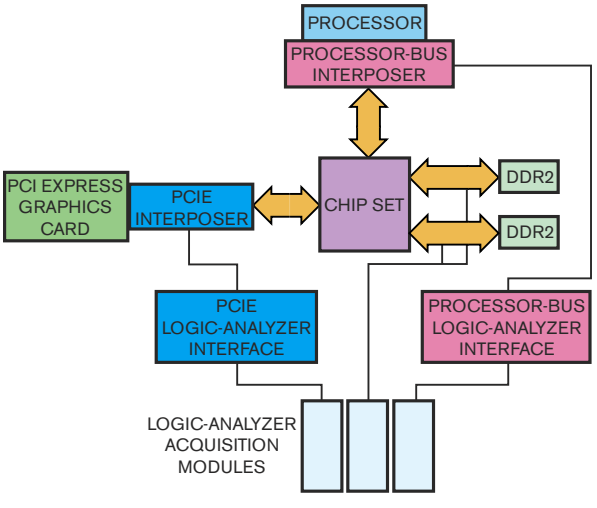


Figure 1 Troubleshooting on the motherboard of a mobile device can involve simultaneous probing of multiple buses of disparate types.

divert signals to a logic analyzer without interrupting the path to the device under test. In the case of a processor-bus interposer, for example, the probe plugs into the CPU's board socket, and the device plugs into a socket on the probe. The interposer must provide a means of attaching a standard heat sink so that the device will operate under normal thermal conditions. Some interposers target use in mobile devices. For example, a probe for SODIMMs (small-outline dual-inline memory modules) commonly finds use in laptops and other compact platforms. This probe provides better signal fidelity than conventional techniques might deliver in densely packed mobile circuits.

In serial-bus architectures, the interposer probe carries the device's signals to a logic-analyzer interface. These interfaces span a range of complexity, depending upon the width, data rate, and protocol of the device under test or bus they are monitoring. The logic-analyzer interface buffers data rates that exceed those of the logic analyzer and fans out serial data to the instrument's innately parallel acquisition channels. If the device under test itself is a parallel device with a compatible data rate, the interface may be unnecessary, but the interposer probe is still essential for accurate signal acquisition.

THE PRACTICE OF SIMULTANEOUSLY PROBING MULTIPLE BUSES, ONCE A LUXURY, IS NOW A NECESSITY.

A midbus footprint is a group of contact pads or a test connector sitting astride a bus trace on the pc board in the middle of the bus. The logic analyzer picks off the signals directly from the trace, gaining the advantages of lower capacitive loading and better signal fidelity. The needs of mobile platforms call for flexibility in probing. The same laptop motherboard may require two interposers on two buses, a midbus footprint on another, and simple clip-on leads for a component elsewhere on the board. All of these probe media will be in action at the same time. Compactness and accurate delivery of signals from all of these multiple buses are essential.

## WAITING FOR THREE BUSES AT ONCE

The practice of simultaneously probing multiple buses, once a luxury, is now a necessity. Time-to-market pressures have driven designers to seek troubleshooting approaches that quickly yield actionable answers. Designers have discovered that the best way to trace a problem often involves triggering on the error while viewing its origins in one subsystem and its consequences in another. Interactions and dependencies among buses that are not electrically connected can reveal much about a system's stability.

Suppose a prototype for a new laptop motherboard has emerged from fabrication and, during design validation, regularly encounters problems in its routine functional exercises. In the worst case, the device freezes and requires rebooting. In other instances, the device seems to operate normally, but the display is garbled and meaningless.

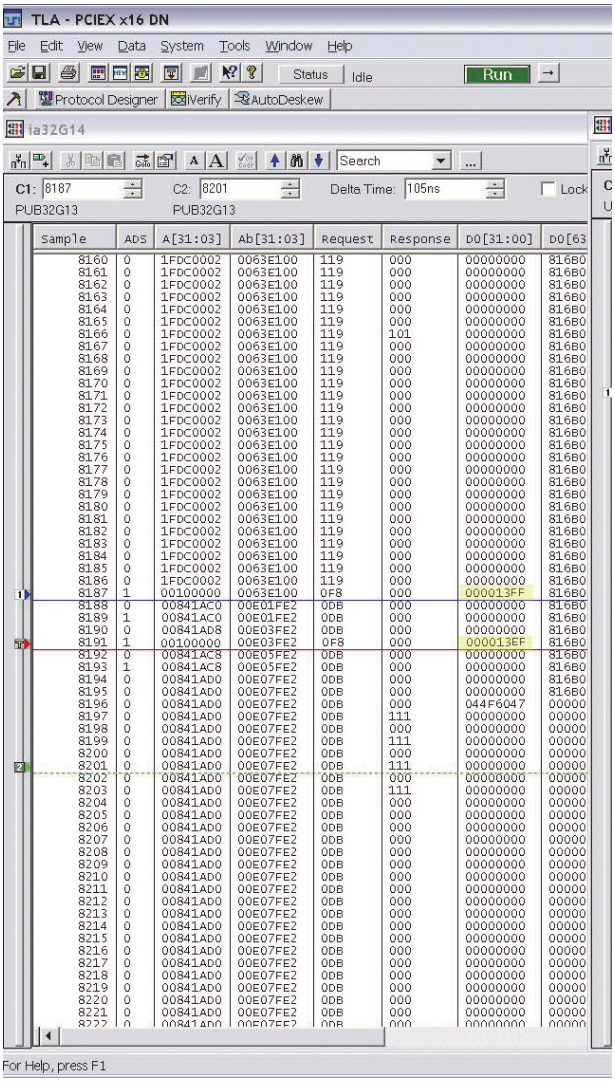


Figure 2 The hexadecimal data acquired from the PCI Express bus implies that the error did not originate on this bus.

Assume that this exercise is a deliberate validation test, not an online operation. The test proceeds as follows: First, the CPU issues a write command and sends data 13FFh to an address location in the DDR2 (double-data-rate 2) memory. Looking at **Figure 1**, the instruction follows an obvious path: from CPU through the processor bus to the chip set and ultimately through the DDR bus to the memory devices. Then the graphics card issues a read command targeting the same address. The command goes over the PCI Express bus, through the chip set, and to the DDR2 memory. Lastly, the CPU issues a second write command and sends new data to the same location in the DDR2 memory.

Because no other instruction should have modified the data before the read, the result of the query should be 13FFh—exact-

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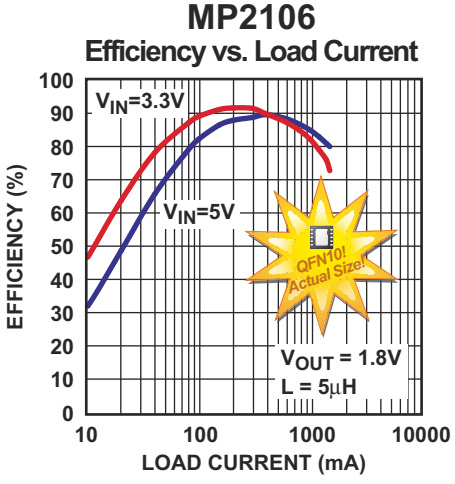


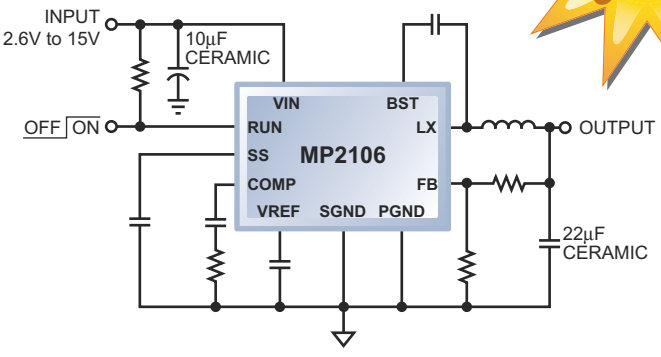


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| MP2305 | 340kHz | 4.75 - 23 | 2.0 | SOIC8 |
| MP1570 | 340kHz | 4.75 - 23 | 3.0 | SOIC8 |
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| MP1593 | 385kHz | 4.75 - 28 | 3.0 | SOIC8 |

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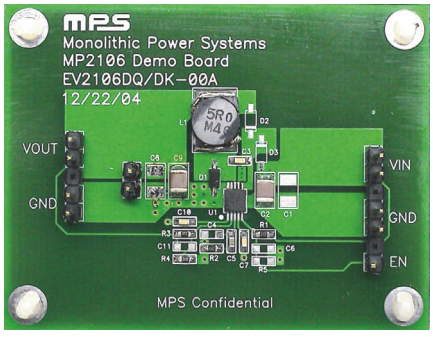


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ly the same data that was written during the first cycle. But the result is 13EFh, and the PCI Express card reports an error. The fastest and easiest way to track down the problem is to simultaneously monitor all three of the buses involved in the transaction. In **Figure 1**, logic-analyzer units connect the PCI Express-bus and processor-bus interposers to logic-analyzer acquisition modules, and a midbus probe brings the DDR2 data directly to a group of logic-analyzer channels.

## PARALLELIZING SERIAL DATA

Looking at the transactions from the PCI Express bus in their parallelized form that the logic-analyzer interface delivers, it becomes clear that the PCI Express graphics card is receiving the incorrect 13EFh data word; it is accurately reporting flawed data (**Figure 2**). Neither the graphics card nor the PCI Express bus is the source of the problem. The next step is to look at the DDR2 bus. Here, a read operation confirms that the bus wrote the correct address, which brings the processor into question. Did it send the data it was supposed to send? Monitoring the processor bus via its interface box establishes that the processor wrote the correct data to memory. All three buses seem to be doing their jobs correctly, and the CPU is correctly issuing data and sending it to the desired memory location. The only remaining possibility is a timing conflict. One potential suspect is the read/write timing. Yet the previous steps have established that the CPU is issuing the write command at the expected time.

For suspicious timing and synchronization problems, the logic analyzer's ability to display correlated traces from all three buses is a time-saver. A look at the memory bus reveals that the second write cycle precedes rather than follows the read (**Figure 3**). The PCI Express card thus receives data stored one operation *later* than intended. The time-correlated view of the read, write, and data values on respective buses reveals a classic problem: The chip set, which should act as a traffic director, is incorrectly timing the graphics card's read request. The read fails to access the memory after the first CPU write cycle as intended.

## TRACKING FAULTS

Laptop computers implement a sleep mode wherein elements other than the system memory power down during periods of inactivity. The objective is to conserve battery energy. When the device wakes up from this mode, it should come back to life and immediately be ready for use. But suppose that the laptop freezes during its attempt to resume regular operation. A logic analyzer can trace the conditions that caused this failure.

After connecting an interposer, troubleshooting begins with an examination of the last valid transactions on the processor bus. Disassembly software residing on the logic analyzer converts the raw hexadecimal data into the human-readable instructions of the original development language. As a result, you see that the code-fetch instructions become corrupt. The actual data may comprise legitimate codes that are incorrect in this context or may contain random sequences that the disassembler simply can't interpret.

The next step is to view the memory bus to see whether

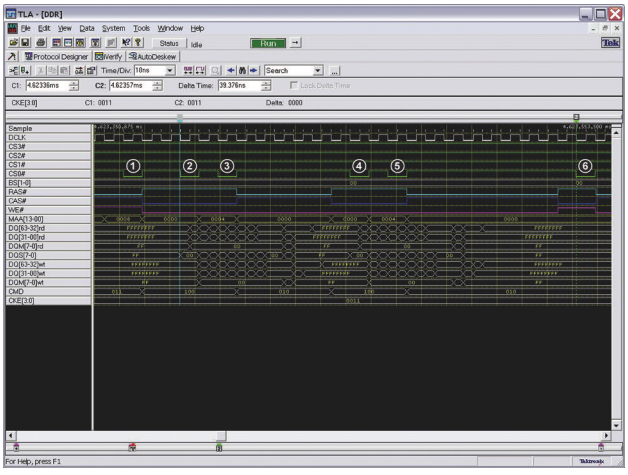


Figure 3 On the DDR bus, after CS0-1 opens the row, a sequence of write operations occurs, commencing after the cursor. CS0-2 and CS0-3 are the first actual writes to the memory in this sequence. The paired pulses write to consecutive addresses. CS0-4 and CS0-5 are two writes. CS0-6, the final command to this address location, is a read command that should be occurring *before* the CS0-4 and CS0-5 pair.

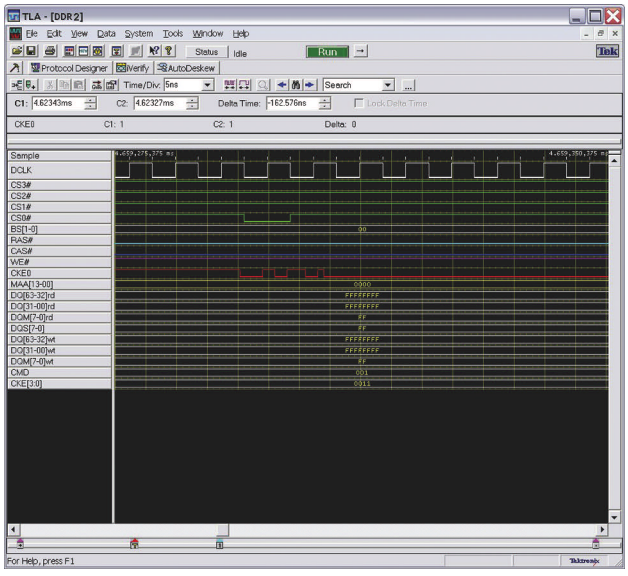


Figure 4 A timing view of the events preceding the transition to sleep mode shows that the CKE0 signal contains several glitches that are causing memory-refresh problems.

the chip set is altering code fetches as they pass through it. If the system-memory data matches that on the processor bus—that is, if the data still contains the corrupted fetch instructions—then the chip set's data transfer is not at fault. This condition implies that the data degraded while it was in the memory during sleep mode or that incorrect data was

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stored before the sleep mode began. If the logic analyzer offers appropriate triggering features, it is simple to determine whether the data was correctly stored to begin with. With a trigger condition stipulated, the instrument acquires transactions only when valid, active transactions occur. The logic analyzer captures data both before and after the sleep state, no matter how long that state lasts. If the incoming data is correct, then the only possible conclusion is that the information was corrupted while waiting in memory during the sleep mode.

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## TIMING VIEW REVEALS GLITCH

The logical suspect is the CKE (clock-enable) signal, a common chip-set feature that puts the system memory into sleep mode. Further examination of the CKE0 signal reveals that it experiences momentary glitches as it signals the memory devices to enter sleep mode (**Figure 4**). The timing view that the logic analyzer acquires makes these glitches clear. The glitches unintentionally disable the self-refresh and allow the memory chips to "forget" their data. Although the chip set isn't to blame for transferring incorrect data, it is at fault for creating the failing condition in the first place.

In this example, the logic analyzer's triggering facilities simplify the capture of events that are widely separated in time, whereas multibus probing saves time when a system must acquire signals from diverse buses. With the aid of these tools, the troubleshooting process moves quickly from a theory to a conclusion.

Densely populated mobile system boards present hundreds or thousands of signals to the logic analyzer. More often than not, a problem in a mobile prototype impacts several subsystems. Simply connecting to all these tiny test points is a major challenge, as are triggering, acquiring, and displaying time-correlated results from multiple buses. The logic analyzer must provide tools that speed and simplify troubleshooting, especially by addressing unique problems, such as space constraints driven by product miniaturization and the increasing use of low amplitude/low-power signals to preserve battery life. EDN

## AUTHOR'S BIOGRAPHY

*Kris Utermark is a product-support engineer with more than nine years of experience in the high-tech industry. He currently supports preprocessor-bus tools and aids in developing technical-marketing materials for new bus tools for the logic-analyzer-product line at Tektronix Inc (Beaverton, OR). He holds a bachelor's degree in computer engineering from the University of Illinois—Urbana-Champaign. In his spare time, he enjoys playing and watching sports and playing with his new daughter.*

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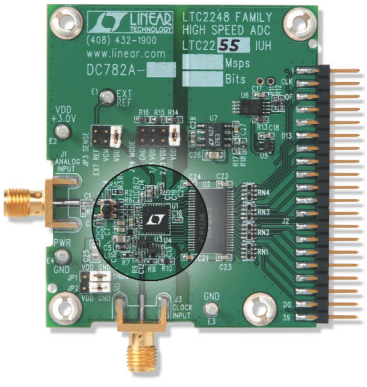


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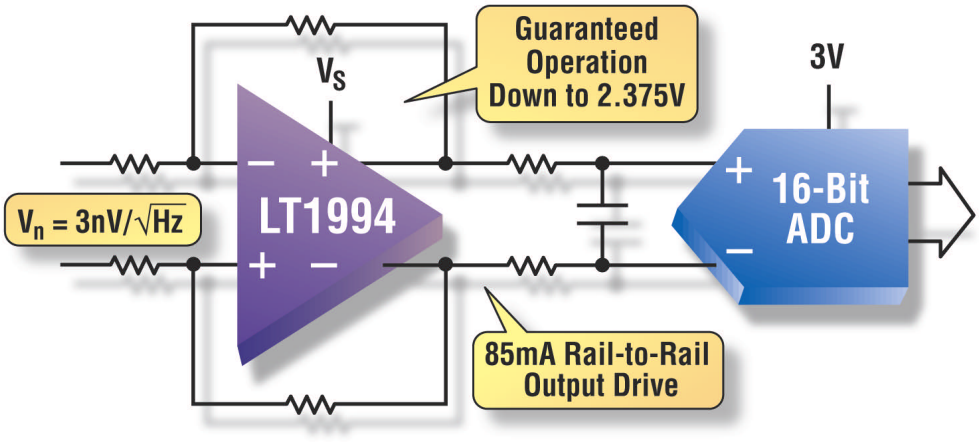


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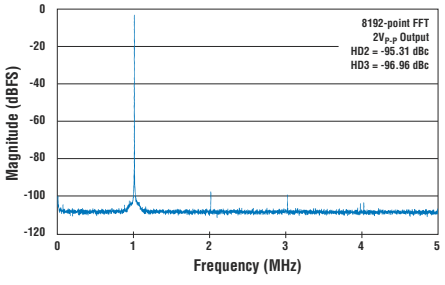


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# designideas

READERS SOLVE DESIGN PROBLEMS

## Audio-test accessory isolates and matches loads

Richard M Kurzrok, RMK Consultants, Queens Village, NY

Connecting a 600Ω audio circuit to a 50 or 75Ω circuit or test instrument requires an impedance-matching circuit or, when isolation of the circuits is necessary, a transformer. Both approaches offer advantages and disadvantages. A conventional transformer can match impedances with low typical losses of 1.5 dB, provide dc isolation, and operate from either a balanced or an unbalanced, 600Ω primary circuit. A high-quality transformer's passband can accommodate an audio-frequency range of 300 Hz to 15 kHz with minimal amplitude variation. However, transformers that can match 600 to 50 or 75Ω may not be readily available or may command a cost premium.

A minimum-loss, fixed-value impedance-matching circuit, or pad, provides frequency-invariant audio-impedance transformation and can comprise as few as two resistors. Although a pad can provide useful impedance matching, it introduces a significant insertion loss of 14.8 dB for a 600-to-75Ω transformation or 16.6 dB for a 600-to-50Ω transformation, either of which might impose an unacceptable loss of dynamic range.

Part of a suite of test accessories, this low-cost, switchable, dual-impedance transformation circuit comprises a single conventional transformer and two minimum-loss pads (**Reference 1**). A single inexpensive, conventional transformer steps down the 600Ω primary input impedance to an intermediate impedance level of 100Ω (**Figure 1**). Switch $S_1$ selects a 100 to 50Ω or a 100 to 75Ω minimum-loss pad. Construction of the unit involves noncritical point-to-point wiring, although this design uses a Hammond 1590LB die-cast-aluminum box to provide shielding and a rugged enclosure to support three Amphenol (www.amphenolrf.com) RFX series BNC panel-mounted, insulated-frame input and output jacks. $T_1$ is a Mouser Electronics (www.mouser.com) 42TM031 audio transformer, and the resistors are 0.5W, metal-film units with ±1% tolerances. With quantity discounts, the overall bill-of-materials cost is less than $20.

To verify frequency response and

**TABLE 1 INSERTION LOSS VERSUS FREQUENCY**

| Frequency (kHz) | Insertion loss (dB) 600 to 50Ω | Insertion loss (dB) 600 to 75Ω |
|---|---|---|
| 0.1 | 11.7 | 8.7 |
| 0.3 | 10 | 7 |
| 0.5 | 9.5 | 6.7 |
| 1 | 9.2 | 6.5 |
| 2 | 9 | 6.3 |
| 5 | 8.9 | 6.1 |
| 10 | 8.8 | 6.1 |
| 20 | 8.8 | 6 |
| 50 | 8.9 | 6.1 |
| 100 | 9.5 | 6.7 |

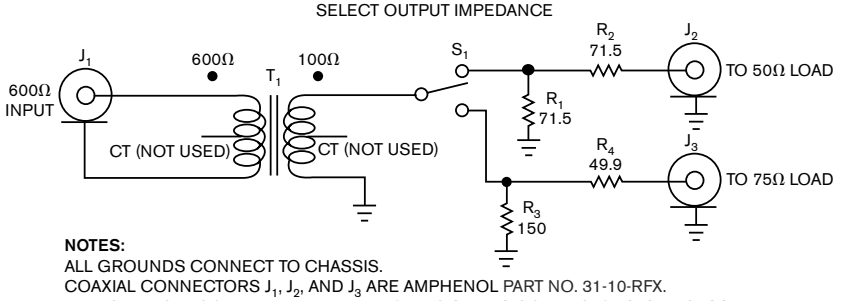


Figure 1 A handful of passive components creates a handy test fixture for matching impedances in audio-test circuits.

### DIs Inside



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attenuation in a 600Ω test setup, connect two identical units back to back through their 50 or 75Ω terminals. You obtain the measured data (**Table 1**) for a single unit by halving the 600-to-600Ω transmission-loss measurements.

Calculated insertion loss for the 100 to 50Ω minimum-loss pad is 7.7 dB, and insertion loss for the 100 to 75Ω minimum-loss pad is 4.8 dB. Subtracting these values from the measured losses indicates that the transformer contributes a midband loss of 1.3 to 1.5 dB. Insertion loss due to stray coupling from the selected output port to an unused output exceeds 40 dB. Combining a conventional transformer with two minimum-loss pads takes advantage of the best of both techniques.

The low-cost transformer contributes moderate insertion losses and provides dc isolation and good frequency response. In addition, the transformer's low-frequency roll-off helps reduce 60-Hz hum and low-frequency noise. The electrically isolated input jack allows connection of the transformer's input to balanced or grounded 600Ω sources. EDN

## REFERENCE

1 Kurzrok, Richard M, "Simple Lab-Built Test Accessories for RF, IF, Baseband, and Audio," *High Frequency Electronics*, May 2003, pg 60.

# One oscillator drives multiple solid-state relays

Juan Ramón Vadillo Pastor, SOR Internacional SA, Saint Quirze Del Valles, Barcelona, Spain

Thanks to a combination of low initial cost and low on-resistance, a conventional electromechanical relay often makes sense for switching large amounts of load current on and off and when proportional control of the load's current or voltage is unnecessary. Low cost and low on-resistance represent the main reasons that relays still enjoy widespread use in the industry. In addition, a relay remains useful for switching high-voltage ac under the control of low-voltage electronics, due to the high degree of isolation between the control and the load circuits.

However, although relay technology has matured and offers proven performance, the relay remains a mechanical device that suffers from wearing out and other failure modes. Electrical endurance of the relay's contacts imposes a limit on the number of switching cycles. When a relay's contact opens, interruption of the current in an inductive load causes a spark that deteriorates the contact's performance. When switching high currents, a relay may reach the end of its operating lifetime in as few as 100,000 actuation cycles.

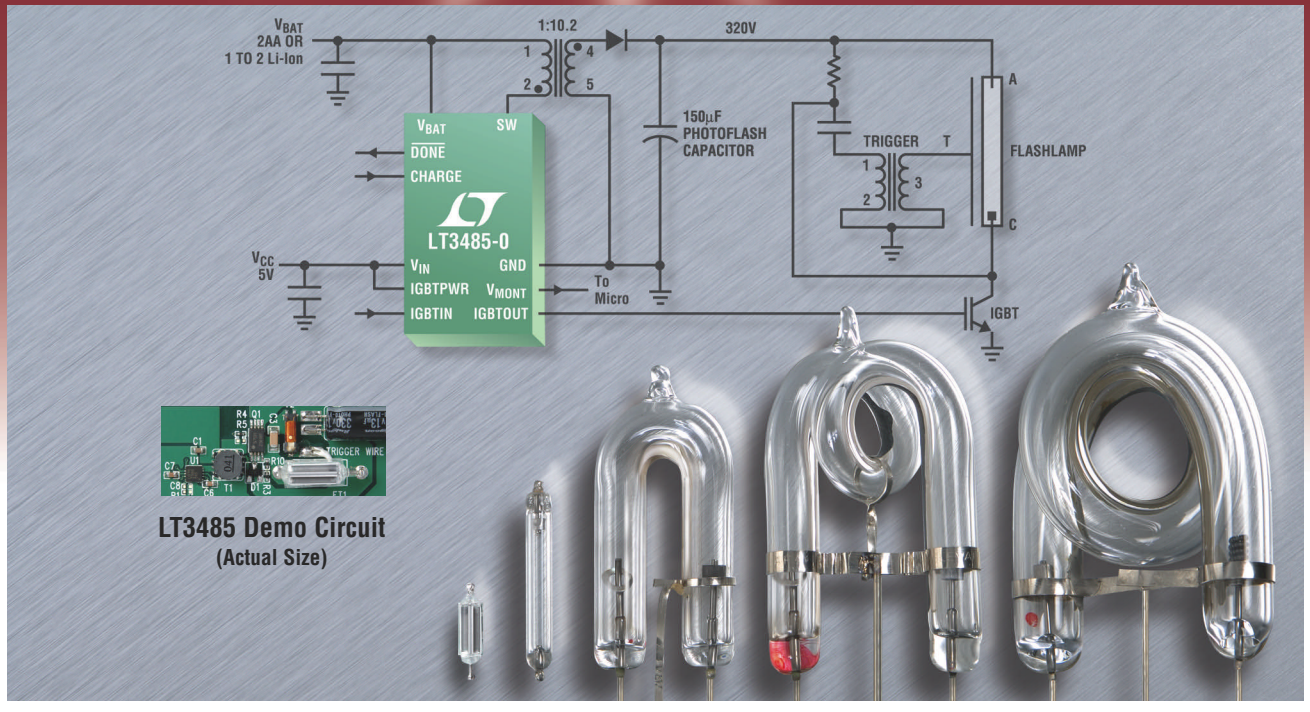
As an alternative to a conventional relay, a series-connected pair of MOSFETs can replace a contact in an ac circuit (**Figure 1**). A pair of IRF530 devices switches loads in circuits with peak maximum voltages as high as ±100V. Based on the well-known 555 timer, an astable oscillator, $IC_1$, provides a source of square-wave voltage to drive the MOSFET pairs' gate. Resistors $R_1$ and $R_2$ provide charge and discharge paths for timing capacitor $C_1$. The 555's output stage can sink and source several tens of milliamperes and provide enough current to drive as many as 10 stages' simultaneously operating switch gates, each consuming 5 mA of peak current; the 555's output sinks a maximum of 50 mA at an on-state maximum voltage of 0.75V. The 555's output drives a distribution bus that provides power to an array of pulse transformers, $T_1$ and $T_2$. Capacitor $C_3$ in series with the transformers' primary removes the dc offset voltage that would otherwise appear across the winding.

Selection of the transformer is not critical, and any ferrite-core pulse transformer that can provide gate voltage to the MOSFETs and maintain a safe level of voltage isolation can function in the circuit. For example, you can use C&D Technologies' (www.cdtech.com) 76601/3, which provides a 1-to-1 turns ratio at a primary inductance of 219 µH with 500V-dc interwinding isolation.

Applying a control signal to the base of general-purpose NPN switching transistor $Q_3$ allows collector current to flow through the primary of its associated transformer. Diode $D_2$ provides a reverse-current path through the winding. On the secondary side, diode $D_1$ rectifies the secondary voltage and charges capacitor $C_4$, which filters the rectified voltage to improve noise immunity and reduce voltage ripple at the MOSFETs' gates. Removing the control signal switches off $Q_1$ and $Q_2$. Resistor $R_3$ provides a discharge path for $C_4$, allowing the MOSFETs to switch off in approximately 3 msec. For faster turn-off, you can reduce the value of either $C_4$ or $R_3$ at the expense of increased ripple on the rectified gate voltage.

Using two series-connected MOSFETs allows bidirectional ac conduction through the pair. When the MOSFETs are off, their parasitic diodes connect in series opposition and thus block conduction. You can select from among a range of MOSFETs to match your application's requirements, but make sure that the voltage you apply to the gates of $Q_1$ and $Q_2$ is sufficient to fully switch

# Flash It!

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| LT3485-0/1/2/3 | 1.8V to 10V | 750/500/350/225mA | 3mm x 3mm DFN-10 |
| LT3420/-1 | 1.8V to 16V | 840/450mA | 3mm x 3mm DFN-10, MSOP |
| LT3750 | 3V to 24V | Up to 4A* | MSOP |

* Controller Depends on External MOSFET selection.

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both devices into full conduction. The IRF530 has a gate threshold voltage of 3V, but applying a gate-source voltage of 10V ensures low on-resistance. You can adjust the gate-source voltage by altering the transformer's turns ratio or $IC_1$'s power-supply voltage within its 4.5 to 16V rating (**references 1** and **2**). EDN

## REFERENCES


1 "Transformer-isolated gate driver provides very large duty cycle ratios," Application Note 950, International Rectifier Co, www.irf.com/technical-info/appnotes/an-950.pdf.

2 Balogh, Laszlo, "Design and application guide for high speed MOSFET gate drive circuits," Texas Instruments, 2002, focus.ti.com/lit/ml/slup169/slup169.pdf.


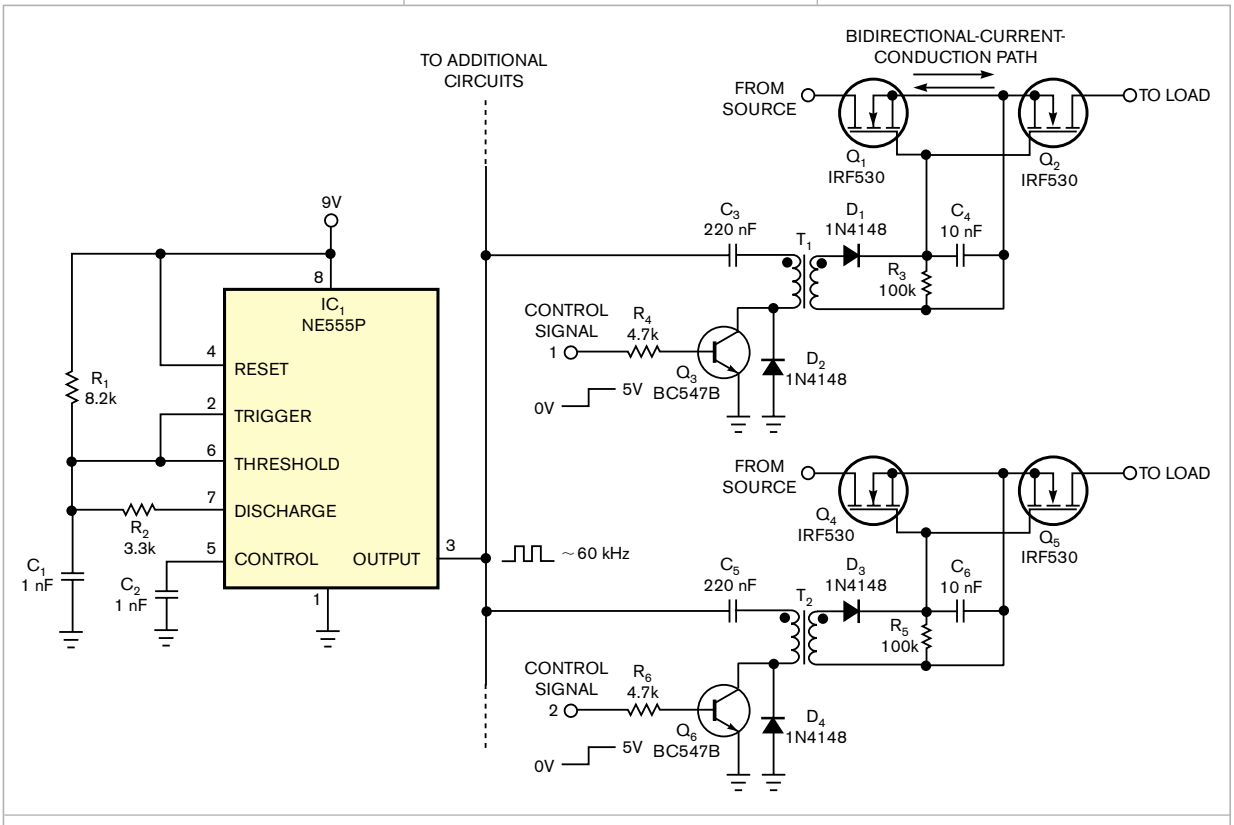


Figure 1 A single 555 oscillator provides square-wave ac gate drive to an array of as many as 15 MOSFET-based solid-state relays.

# Low-dropout linear regulators double as voltage-supervisor circuits

William Lepkowski, On Semiconductor, Tucson, AZ

Many low-dropout voltage regulators include an enable-input pin that can also serve as an inexpensive alternative to a voltage-supervisor IC. Although the enable pin normally serves as a means of shutting down the regulator's output to save power, a few discrete components ensure that the regulator's output will turn on and off at appropriate input voltages. Thus, you can use the circuit as a voltage supervisor or as a controlled-characteristic linear-voltage regulator.

A typical low-dropout regulator's internal enable circuit comprises a voltage comparator that determines whether the voltage at the enable pin is either larger or smaller than an internal reference voltage, $V_{REF}$. Although you can create a low-dropout voltage supervisor by directly connecting the enable pin to the unregulated input voltage, this circuit's turn-on and turn-off voltages equal the reference voltage, which typically falls below the minimum operating voltage that most ICs powered by the regulator's output require.

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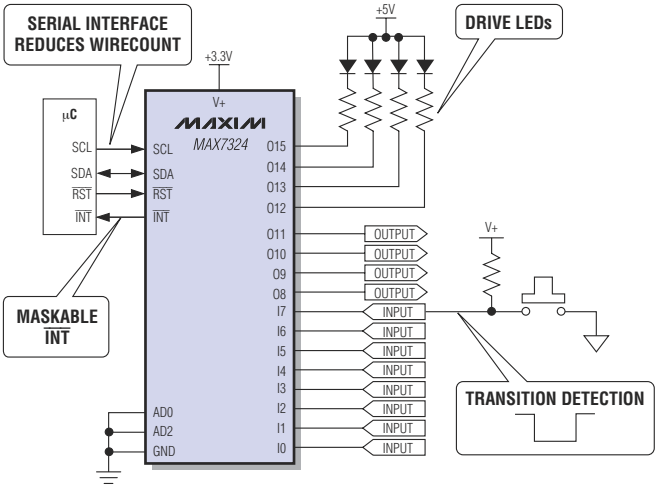


| Part | $\overline{RST}$ Input | No. of Inputs | Interrupt Mask | No. of Open-Drain Outputs | No. of Push-Pull Outputs | Package |
|---|---|---|---|---|---|---|
| MAX7319 | ✓ | 8 | ✓ | – | – | 16-QSOP/TQFN |
| MAX7320 | ✓ | – | – | – | 8 | 16-QSOP/TQFN |
| MAX7321 | ✓ | Up to 8 | – | Up to 8 | – | 16-QSOP/TQFN |
| MAX7322 | ✓ | 4 | ✓ | – | 4 | 16-QSOP/TQFN |
| MAX7323 | ✓ | Up to 4 | – | Up to 4 | 4 | 16-QSOP/TQFN |
| MAX7328* | – | Up to 8 | – | Up to 8 | – | 20-SSOP/16-W-SO |
| MAX7329** | – | Up to 8 | – | Up to 8 | – | 20-SSOP/16-W-SO |
| MAX7324 | ✓ | 8 | ✓ | – | 8 | 24-QSOP/TQFN |
| MAX7325 | ✓ | Up to 8 | – | Up to 8 | 8 | 24-QSOP/TQFN |
| MAX7326 | ✓ | 4 | ✓ | – | 12 | 24-QSOP/TQFN |
| MAX7327 | ✓ | Up to 4 | – | Up to 4 | 12 | 24-QSOP/TQFN |

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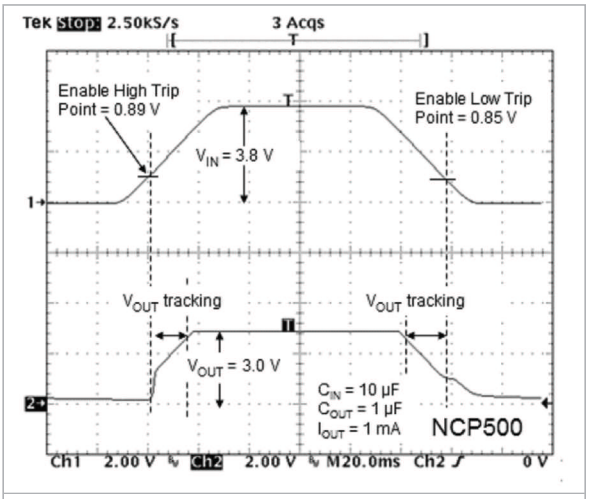


Figure 1 Connecting a low-dropout regulator's enable pin directly to the unregulated voltage input forces the output voltage to track the input voltage during the regulator's turn-on and turn-off intervals.

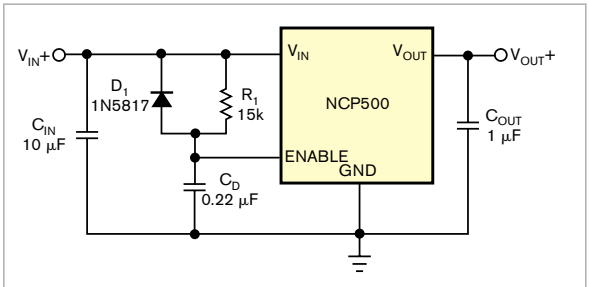


Figure 2 An alternative to directly connecting the regulator's input and enable pins, this "conventional" modification uses a resistor and a capacitor to delay the regulator's turn-on time. The diode eliminates the power-down delay interval.

In addition, directly connecting the enable pin to the unregulated input doesn't provide a turn-on delay to ensure that the input voltage has reached a value higher than the low-dropout regulator's dropout voltage. The directly connected circuit has unsatisfactory power-up and power-down characteristics (**Figure 1**). As a first-order improvement, you can enhance the circuit's performance by adding $R_1$, $C_{IN}$, and $D_1$ to provide a start-up delay for the voltage regulator's enable pin (**Figure 2**). Unfortunately, the external delay network improves the output's rising-edge characteristic, but its falling edge continues to track the input voltage (**Figure 3**).

You can solve the circuit's shutdown problem by replacing the single resistor with a voltage-divider network (**Figure 4**). Resistor $R_2$ raises the switching threshold of the regulator's enable pin and "tricks" the enable comparator into turning on at a higher voltage. The regulator's output then exhibits an adequate start-up delay and

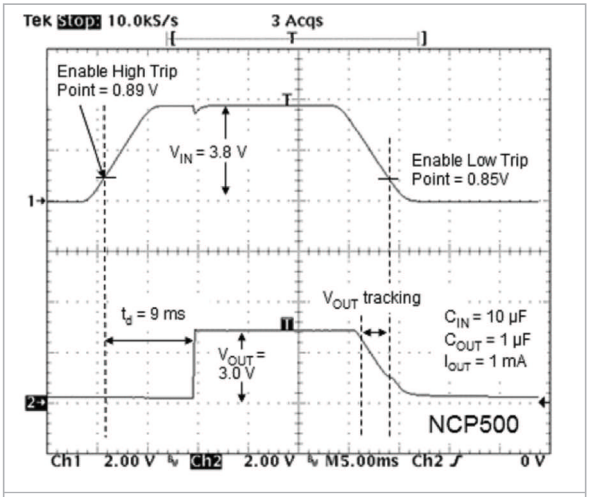


Figure 3 The added components in Figure 2 eliminate the problem of rising-edge output-voltage tracking. However, the falling-edge output voltage still tracks the input voltage.

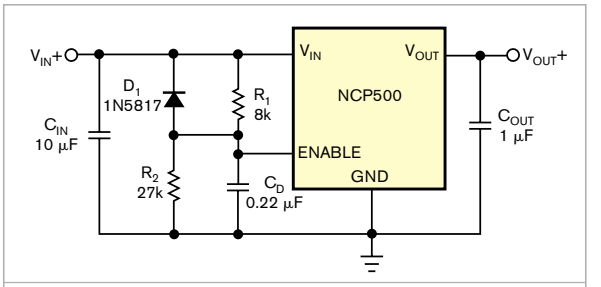


Figure 4 Resistor $R_2$ increases the enable pin's switching threshold voltage.

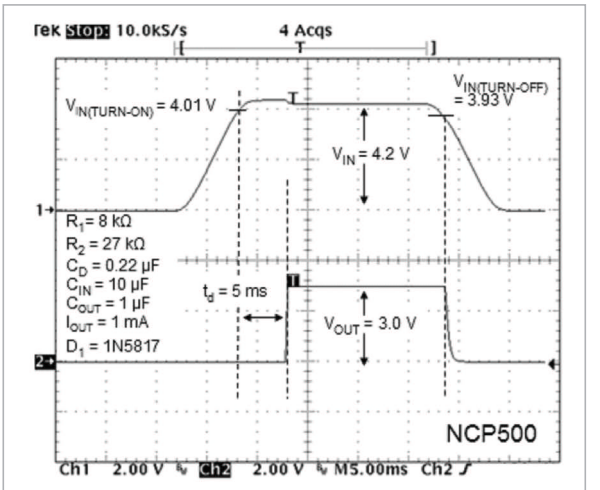


Figure 5 The addition of $R_2$ in Figure 3 solves the falling-edge problem, and shutdown occurs immediately after the input voltage drops too low. The regulator's output switches on only after sufficient voltage is present at its input.

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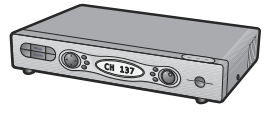


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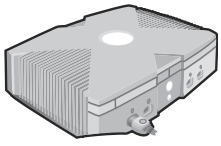
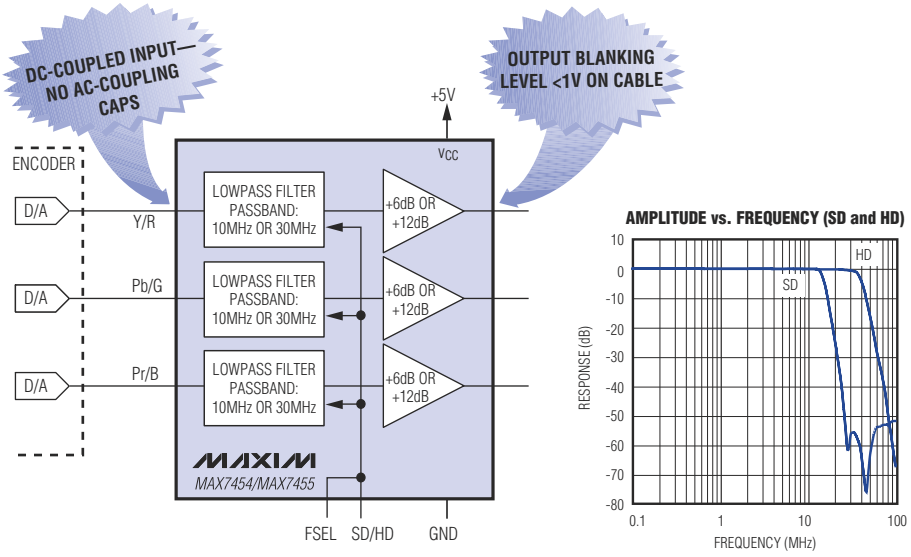


HD GAME CONSOLE

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cleanly switches on and off (**Figure 5**).

You can use **Equation 1** to calculate the values of resistors $R_1$ and $R_2$ to alter the enable pin's threshold voltage in the circuit in **Figure 4**.

$$V_{IN(TURN-ON)} \simeq \left[\left(2\times V_{EN(RISING)}\right)-V_{EN(FALLING)}\right]\times\left(1+\frac{R_1}{R_2}\right), \quad (1)$$

where $V_{IN(TURN-ON)}$ is the user-defined turn-on voltage, $V_{EN(RISING)}$ is the enable pin's rising-edge trip-point voltage, and $V_{EN(FALLING)}$ is the enable pin's falling-edge trip-point voltage. For example, $V_{IN(TURN-ON)}=4V$, $V_{EN(RISING)}=0.89V$, and $V_{EN(FALLING)}=0.85V$. To prevent the regulated output voltage from tracking the input, set the minimum value of $V_{IN(TURN-ON)}$ to $V_{OUT}+V_{DROPOUT}$, where $V_{DROPOUT}$ is the dropout voltage.

$$\frac{R_1}{R_2} \simeq \frac{V_{IN(TURN-ON)}}{\left[\left(2\times V_{EN(RISING)}\right)-V_{EN(FALLING)}\right]}-1 \simeq \frac{4}{\left[\left(2\times 0.89\right)-0.85\right]}-1 \simeq 3.3. \quad (2)$$

If you select a value of 8 kΩ for $R_2$, then $R_1=3.3\times R_2$, or approximately 27 kΩ.

**Equation 1** calculates only approximate values for the voltage-divider resistors, which may vary slightly depending on the voltage regulator's characteristics. If the resistors' values are too low, the regulated output tracks the input, a problem that you can easily solve by increasing the value of $R_1$. Also, $R_1$ and $C_D$ determine the regulator's turn-on delay time, and $C_D$'s capacitance should ideally be 0.01 to 0.47 µF. Too large a value increases the discharge time and reduces the circuit's effectiveness as a voltage supervisor. EDN

# External components provide true shutdown for boost converter

Navid Mostafavi, Maxim Integrated Products Inc, Sunnyvale, CA

The step-up switching-converter circuit in **Figure 1** presents a familiar problem: If you shut down boost converter $IC_1$ by pulling its $\overline{SHDN}$ input low, external inductor $L_1$ and forward-biased Schottky diode $D_1$ allow the load to continue drawing current. For battery-powered applications that present a heavy load—300 mA, for example—this unwanted dc-current path may quickly drain the battery. Adding an N-channel MOSFET, $Q_1$, and a 100-kΩ resistor, $R_1$, solves the problem by opening the unwanted current path during shutdown. The resulting circuit is suitable for battery-powered-system applications in which a microcontroller handles the power management.

Asserting a low logic level on the $\overline{SHDN}$ input simultaneously shuts down the switching converter, a MAX756, and turns off the MOSFET, thereby blocking load current by removing the load's ground connection. When the $\overline{SHDN}$ signal deasserts, the 100-kΩ pullup resistor turns on the MOSFET by pulling the MOSFET's gate high. With its ground reconnected, the load then draws current from the activated boost-converter circuit.

For optimum results at high load currents, select a logic-level MOSFET for $Q_1$ that presents a reasonably low on-resistance. The MOSFET's drain-to-source breakdown voltage should also be able to withstand at least twice the maximum output voltage you expect from the boost converter. If necessary, you can reduce the MOSFET's effective on-resistance by connecting two or more MOSFETs in parallel. EDN

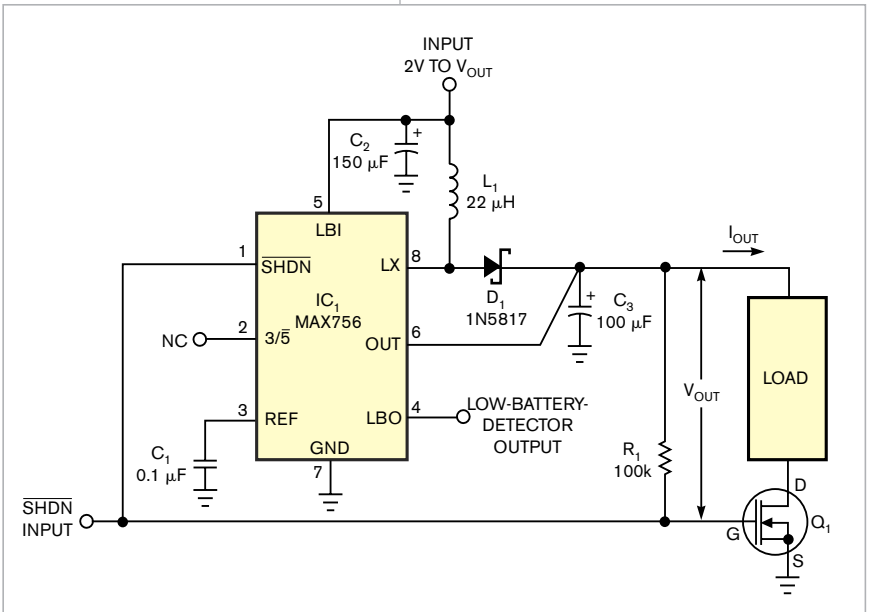


Figure 1 Adding $R_1$ and MOSFET $Q_1$ to this step-up-converter circuit enables the $\overline{SHDN}$ control to impose a "true" shutdown that blocks load current when boost converter $IC_1$ switches off.

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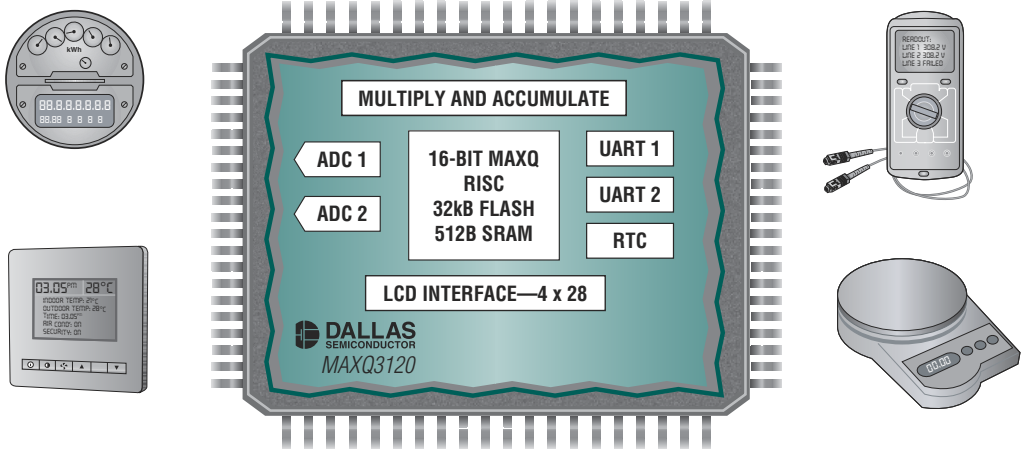


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*(continued on pg 91)*

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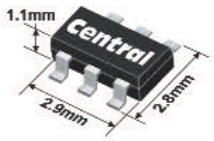


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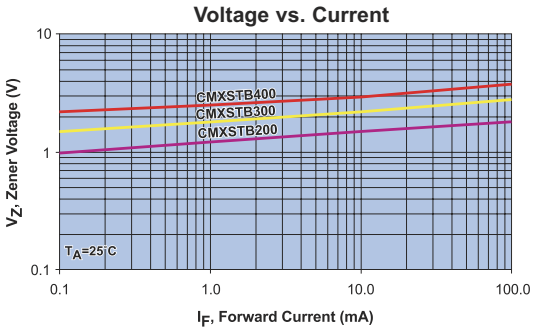


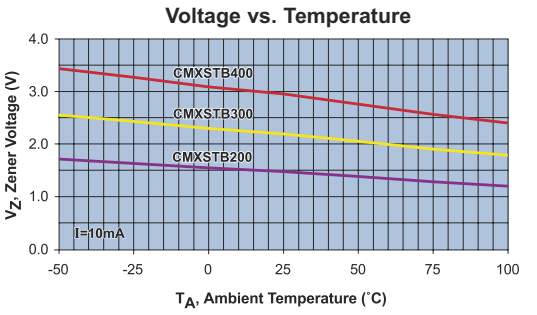


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DESIGN NOTES

# Accurate Power Supply Sequencing Prevents System Damage

Design Note 384

Jeff Heath and Akin Kestelli

## Introduction

Many complex systems—such as telecom equipment, memory modules, optical systems, networking equipment, servers and base stations—use FPGAs and other digital ICs that require multiple voltage rails that must start up and shut down in a specific order, otherwise the ICs can be damaged. The LTC®2924 is a simple and compact solution to power supply sequencing in a 16-pin SSOP package (see Figures 1 and 2).

## How it Works

Four power supplies can be easily sequenced using a single LTC2924 and multiple LTC2924s can be just as easily cascaded to sequence any number of power supplies. With slightly reduced functionality, six power supplies can be sequenced with a single LTC2924.

The LTC2924 controls the start-up and shutdown sequence and ramp rates of four power supply channels via output pins (OUT1 to OUT4). Each OUT pin uses a 10µA current source connected to an internal charge pump and a low resistance switch to GND. This combination makes the outputs flexible enough to connect them directly to many power supply shutdown pins or to external N-channel MOSFET switches.

The LTC2924 monitors the output voltage of each sequenced power supply via four input pins (IN1 to IN4). These inputs use precision comparators and a trimmed bandgap voltage reference to provide better than 1% accuracy. The power ON and power OFF voltage thresholds are set using resistive dividers for each of the four channels. The power ON threshold and the power OFF threshold are individually selectable on a channel by channel basis (see "Selecting the Hysteresis Current and IN Pin Feedback Resistors" in the data sheet for details).

The LTC2924 timer pin (TMR) is used to provide an optional delay between the completion of start-up of one supply and the start-up of the next power supply. The delay time is selected by placing a capacitor between the TMR pin and ground (delay = 200ms/µF), whereas floating the TMR pin removes any delay. The start-up delay can be different than the shutdown delay. Figure 3 shows a simple circuit where the shutdown delay is half the start-up delay.



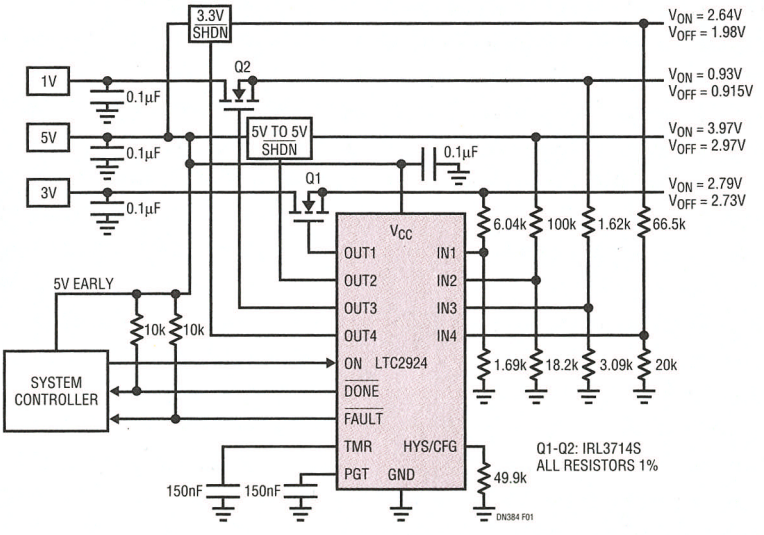


**Figure 1. Typical Application with External N-Channel MOSFETs**

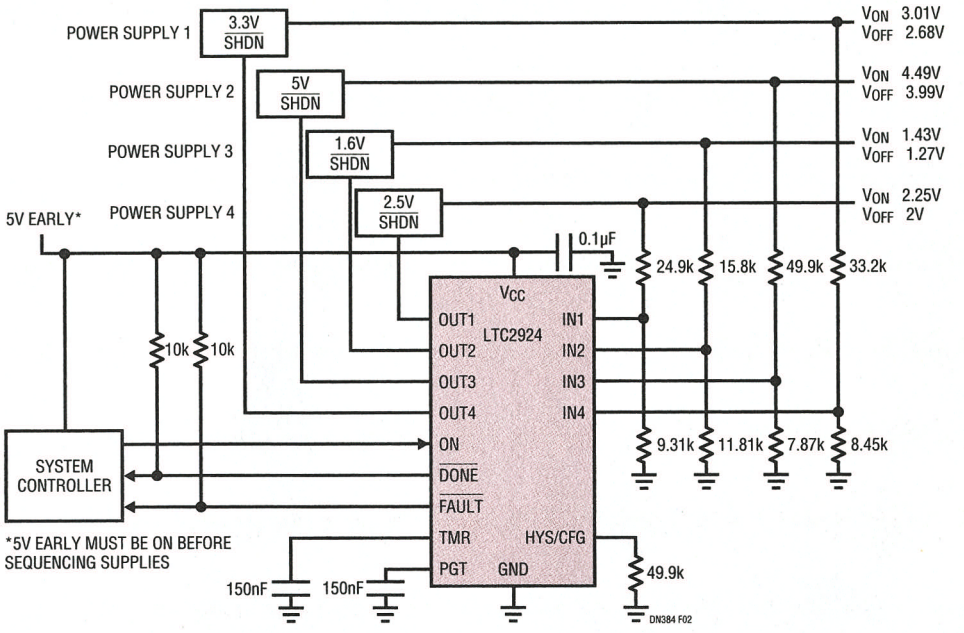


**Figure 2. Four Power Supply Sequencer Using Shutdown Pins**

The LTC2924 also includes a power good timer (PGT). The LTC2924 starts the PGT as each individual power supply is enabled. If any power supply fails to reach its nominal specified voltage within the allotted time interval, a power ON fault is detected.

## Conclusion

The LTC2924 fits into a wide variety of power supply sequencing and monitoring applications. With very few external components and a 16-pin narrow SSOP, an LTC2924-based sequencing solution requires very little board space.

The power supply enable pins require no configuration by the designer, yet are versatile enough to directly drive shutdown pins or external N-channel MOSFETs. Soft-start of power supplies can be achieved simply by adding a capacitor. If the sequencing of more than four power supplies is required, the LTC2924 can be cascaded to sequence a virtually unlimited number of power supplies. Tailoring the LTC2924 to a specific application requires no software and designs can be fine tuned during system integration simply by changing resistor and capacitor values. Ease of design, low component cost, and a small footprint make the LTC2924 an excellent choice for power supply sequencing and monitoring.

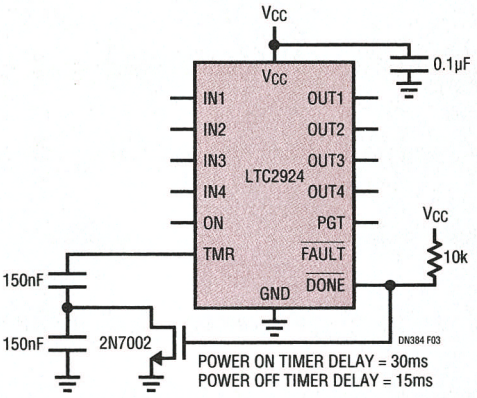


**Figure 3. Programming Different ON/OFF Delays**

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# AMPLIFIERS, OSCILLATORS, AND MIXERS

to simplify board layouts, and has a 2.7V differential output voltage for optical-noise immunity in RS-485/422 networks. The ISL41334 and ISL41387 come in QFN-40 packages; the ISL81334 and ISL-81387 come in SSOP-20 and SOIC-20 packages. Single-port ISL81387 and ISL-41387 transceivers cost $4.60 (1000); dual-port versions of the ISL81334 and ISL41334 cost $5.27 (1000).
**Intersil Corp, www.intersil.com**

## Amplifiers enhance digital-television-audio performance

These two stereo Class D audio-power amplifiers suit digital televisions, including DLP HDTV, LCD, and plasma displays. Features include Class D operation, pop/click-minimizing circuitry, low total-harmonic distortion, and high SNR. Targeting 27-in. and larger digital televisions, the TPA3100D2 drives 20W per channel of continuous stereo-output power with no external heat sink. Aiming at digital televisions smaller than 27 in., the TPA3101D2 provides 10W-per-channel output power. Both devices drive a 4Ω nominal load and come in 7×7-mm quad-flat, lead-free QFN-48 packaging. The TPA3100D2 and TPA3101D2 cost $3.50 and $3.10 (100), respectively.
**Texas Instruments, www.ti.com**

# EMBEDDED SYSTEMS

## Microstepping drive accepts commands over communications network

The Ion microstepping digital drive supports two-phase bipolar motors and automatically switches between user-defined current modes. With a 256 microstep/step-programmable resolution, the drive provides RS-485 asynchronous-serial or CANbus-network communications. Selectable profiling modes include S-curve, trapezoidal, velocity contouring, and electronic gearing. Able to accept position, velocity, and acceleration and jerk commands over communications networks, the device generates a corresponding trajectory on the fly. Available in dc-brush, brushless-dc, and microstepping configurations, the Ion microstepping digital drive costs $223.
**Performance Motion Devices, www.pmdcorp.com**

## Rugged 6U VME unit uses two 1.6-GHz processors

A 6U VME clone of the IBM JS20 blade design, the PowerNode5 comes in convection-cooled and rugged-conduction-cooled versions for harsh environments. Features include two 1.6-GHz IBM 970FX processors and 2 Gbytes of DDR SDRAM ECC memory with 6.4-Gbyte/sec memory-peak bandwidth. These features enable a user to develop applications on a standard IBM blade server and port the application to the device. Support for Red Hat Linux SMP BSP promotes software productivity. The PowerNode5 is available as a board component or as the PowerMP5, preintegrated in large systems, both with data-transport and -management software based on MPI and HTTP standards. The device runs on Red Hat Linux or Wind River VxWorks. Additionally, the device includes two Gigabit Ethernet ports and an onboard serial RapidIO switch fabric allowing a user to build a powerful and scalable signal-processing calculator based on the device's building blocks. The PowerNode5 costs $11,260, depending on configuration.
**Thales, www.thalescomputers.com**

## Tool suite simplifies 8-bit-system application development

Targeting HC(S)08 microcontrollers Version 5.0, the CodeWarrior Development Studio comprises 8-bit Fast Track CodeWarrior development tools. These tools suit ANSI C/C++ and compact C++ compilers and include more than 60 advanced optimization strategies for boosting performance and reducing code size for the HC(S) architecture. The UNIS device-initialization tool provides an easy method of configuring and generating initialization code and adding that code directly to the project or creating a separate text file. Additional features include an improved project wizard with on-screen help functions; a graphical, source-level debugger; support for HC(S)08 on-chip trace and flash programming; full-chip and data visualization; and animated tutorials. The tool suite also includes the UNIS Processor Expert with Bean Wizard and components for HC(S)08 CPUs. The CodeWarrior Development Studio is available in standard and professional editions for $2394 and $4794, respectively.
**Freescale Semiconductor, www.freescale.com**

## 6.4-in. LCD-panel computer incorporates a 667-MHz processor

The ARP-2606AP panel computer incorporates a 6.4-in. LCD, a 3.4-in. embedded board, and the 667-MHz Via Eden processor. System memory includes an SO-DIMM-144 socket with 512 Mbytes of memory. The LAN uses a Relateck8139C PCI plug-and-play BaseT Ethernet controller. Video support features a built-in VGA controller with 32 Mbytes of shared memory. The ARP-2606AP costs $1000.
**Arista Corp, www.aristaipc.com**

# INTEGRATED CIRCUITS

## Image-system controller supports a two-camera subsystem

Based on the vendor's STV0984 image-system controller, the two-camera subsystem supports two SMIA-compliant sensors. Mounted on the face, toward the user, the lower resolution camera is dedicated to video conferencing, and the high-resolution still-image-centric device faces away from the user. The STV0984 imaging-system controller and the VS-6750S02F fixed-focus, 2M-pixel-camera module cost $4.50 and $13, respectively (50,000). The VA6750S02F autofocus variant of the 2M-pixel-camera module costs $18 (50,000).

**STMicroelectronics, www.st.com**

## Processors decode a variety of audio-compression formats

Targeting the car-audio market, the TC94A70-FG and TC94A73MFG use a single-chip, cd-MP3 processor. Both devices feature 1 Mbyte of SRAM; the TC94A73MFG adds a system-in-package version, including ESP (electronic-shock protection), by adding built-in firmware and 16 Mbytes of DRAM. The TC94A73FG-002 can decode MP3, WMA9, and ATRAC (Adaptive Transform Acoustic Coding) CD; the TC94A73FG-005 can decode MP3, WMA-9, ATRAC CD, and AAC. The TC94A73MFG-201 can decode MP3 and WMA9, and it includes the ESP feature; the TC94A73MFG-201 can decode MP3, WMA9, ATRAC CD, and AAC, and it includes the ESP feature. The TC94A-73FG line and the TC94A73-MFG line cost $7 and $9 (10,000), respectively.

**Toshiba America Electronic Components Inc, www.toshiba.com**



## Codec features Class D stereo-speaker driver

Delivering 1W continuously, the WM8960 stereo codec suits portable electronic devices including mobile phones with stereo speakers and personal video players. Features include a filterless, Class D stereo-speaker driver, stereo ADCs and DACs, a headphone driver, and an internal PLL. The WM-8960 comes in a QFN package and costs $2.98 (10,000).

**Wolfson Microelectronics, www.wolfsonmicro.com**

## Stereo-audio ADCs come in small package

Available in lead-free TSSOP-10 packages, the CS5343 and CS5344 stereo-audio ADCs measure 15×15 mm. The CS5343 supports the I²S format; the CS5334 supports the left-justified serial data format. Each device costs $1.35 (10,000).

**Cirrus Logic, www.cirrus.com**

## Receiver combines dual tuners and demodulators

Integrated dual tuners and demodulators allow the BCM7401 dual-DVB-S2 receiver to fit into an MQFP-208 package, minimizing the number of components in the receiver design. Targeting digital-satellite-broadcast equipment, the device creates a seamless interface to the vendor's BCM7400, BCM7401, and BCM7402 ACV/MPEG-2/VC-1 single-chip devices, as well as the BCM7038/BCM-7411 decoder chip sets. The BCM4501 DVB-S2 satellite-receiver chip costs $25 (1000).

**Broadcom, www.broadcom.com**

## Processor family adds pin-compatible device for mobile devices

Adding to the Nomadic processor family targeting mobile-multimedia devices, the STn8815 adds Level 2 cache to the ARM9 CPU, a smart-imaging accelerator, and memory. The device comes in a 14×14-mm BGA package and features pin compatibility with the previous-generation STn-8810. Available in volume production in the fourth quarter of 2006, the STn8815 costs $19 (10,000).

**STMicroelectronics, www.st.com**

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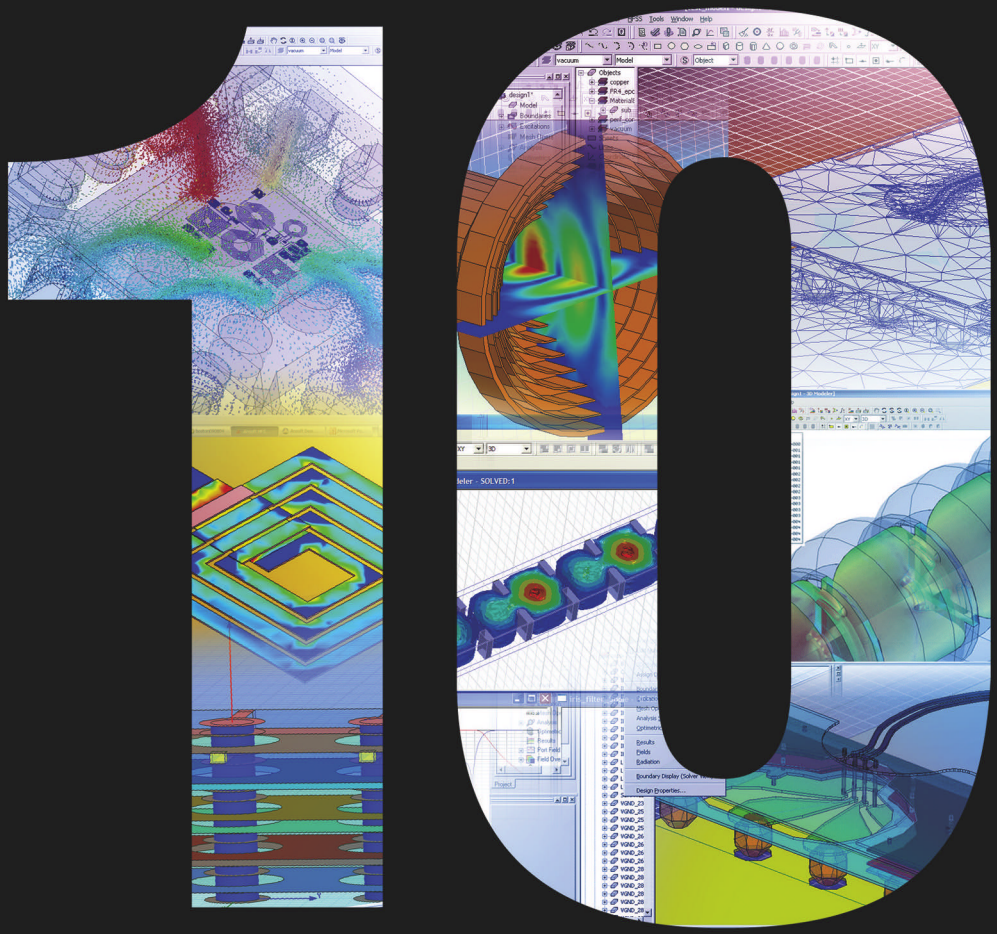

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# Game-console developer transforms itself

Infinium Labs, founded in 2002, spent its first two years of public life fending off repeated and persistent accusations of financial infidelities. The company hit the 2004 Electronic Entertainment Expo show with functional hardware and a full tank of hype. The Phantom Gaming Console, an AMD- and Nvidia-based, PC-derived system conceptually similar to Microsoft's first-generation Xbox, ran an embedded variant of Windows XP and embraced a direct-download, subscription-optional content-delivery model. And the company had significantly boosted its pedigree four months earlier by hiring Kevin Bachus, previously one of the key figures in developing both the DirectX multimedia API and the Xbox at Microsoft, as president and chief operating officer.

Then … nothing. The promised ready-for-Christmas-2004 production schedule came and went, as did a revised March 2005 production date. Company founder Tim Roberts left in mid-2005. The company subsequently named Bachus chief executive officer, but he left the job after only three months. Now, after a $5 million cash infusion, the company intends to significantly scale back its hardware plans and later this year release a gamer-targeted, lap-friendly keyboard-plus-mouse combo.

Will the Phantom Lapboard really appear? And, if so, will the earnings and profit Infinium Labs obtains from it be sufficient to bootstrap the Gaming Console, which the company is still showcasing on its Web site, beyond its current Phantom status?—by Brian Dipert

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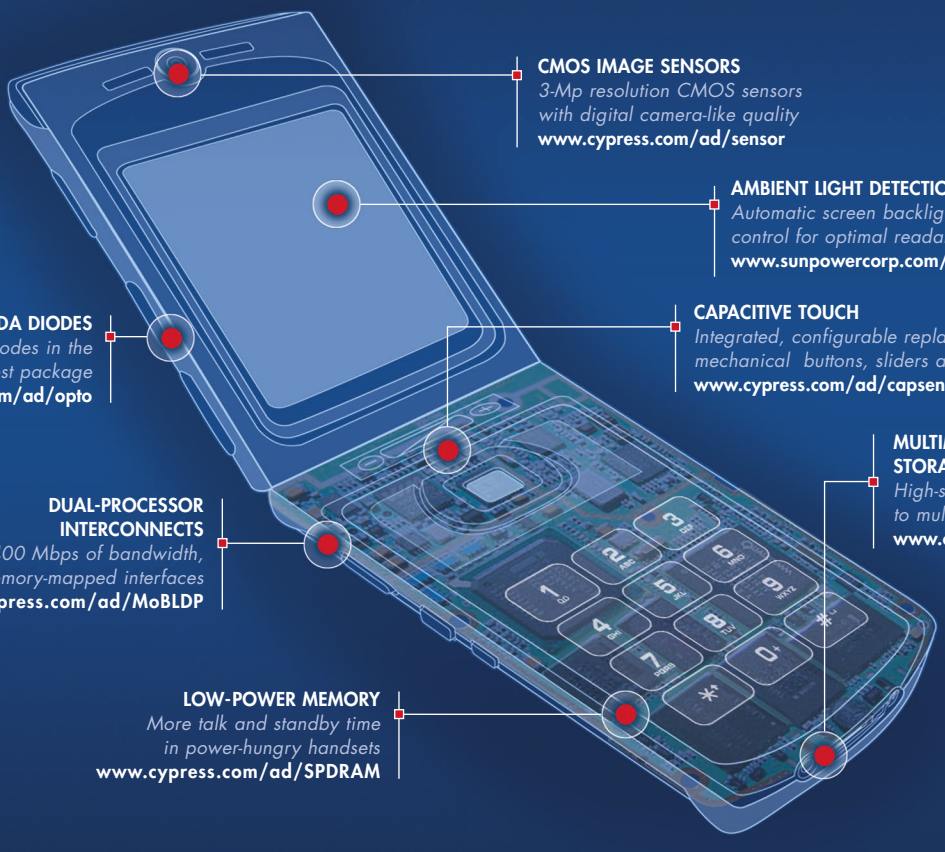

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